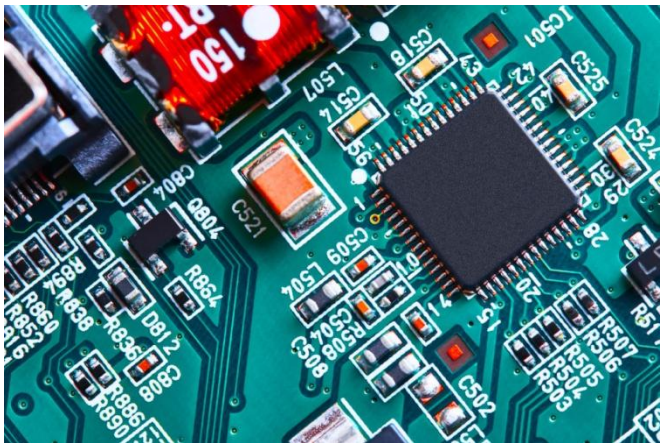
PURNEA COLLEGE OF ENGINEERING
PURNEA

COURSE FILE

OF

DIGITAL ELECTRONICS

(100403)



Faculty Name:

Mr. Tabish Shanu
Assistant Professor
Department of Electrical Engineering

VISION & MISSION OF THE INSTITUTE

Vision of The Institute

To consistently strive for excellence in engineering education by producing skilled, trained and knowledge-driven engineers who fit into the current and future requirements of industries, organizations, and society thereby contributing to the sustainable growth of the country.

Mission of The Institute

M1: To improve teaching-learning process while making the existing curriculum more contemporary and in keeping with the requirements of the industry.

M2: To create an environment for fostering research and development.

M3: To develop students' soft skills, ethical values, leadership qualities, reasoning and analytical abilities and motivate them to address engineering needs of neighboring area.

VISION & MISSION OF THE DEPARTMENT

Vision of the Department

To produce competent electrical engineers with ethical values addressing the challenges in the field of education, industry, and research for the sustainable growth of nation.

Mission of the Department

M1: To create an environment for quality technical education and produce engineers who will contribute meaningfully to the growth and development of the country.

M2: To engage the students in research & development in cutting edge and sustainable technologies.

M3: To develop professional skills, ethical values, and leadership qualities to address the needs of neighbouring areas in terms of engineering and technical support.

Programme Outcomes (PO)

PO1	**Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO2	**Problem analysis:** Identify, formulate, review research literature, and analyse complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO3	**Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO4	**Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO5	**Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.
PO6	**The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO7	**Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts and demonstrate the knowledge of and need for sustainable development.
PO8	**Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO9	**Individual and teamwork:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO10	**Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO11	**Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12	**Life-long learning:** Recognize the need for and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PEO (Program Educational Objective)

Graduates of the program will be able to:

PEO1: Establish their careers in the field of Electrical Engineering and related areas, providing innovative and effective solutions.

PEO2: Establish themselves as entrepreneur, work in research and development organization and pursue higher education.

PEO3: Manage projects catering to current societal and industrial needs in an ethical manner as a member/leader of multidisciplinary teams.

PSO (Program Specific Outcome)

Upon satisfactory completion of the program, a student will be able to:

PSO-1: Identify, analyze, and solve real-life problems by applying the knowledge in Electrical Engineering.

PSO-2: Design and develop electrical systems with the help of automation tools to excel in the field of Electrical engineering.

PSO-3: Find solutions to the issues faced by society through engineering and technological innovations while upholding professional ethics and social values.

COURSE OBJECTIVE AND COURSE OUTCOMES:

Institute / College Name :	Purnea College of Engineering		
Program Name	**B. Tech (Electrical Engineering)**		
COURSE CODE	100403		
COURSE NAME	**DIGITAL ELECTRONICS**		
Lecture / Tutorial / Practical (per week):	3-1-2	**Course Credits**	4
Course Coordinator Name	Mr. Tabish Shanu		

Course objective:

The objective of this course is to provide the fundamental concepts associated with the digital logic and circuit design. To introduce the basic concepts and laws involved in the Boolean algebra and logic families and digital circuits. To familiarize with the different number systems, logic gates, and combinational and sequential circuits utilized in the different digital circuits and systems. The course will help in design and analysis of the digital circuit and system.

Course outcomes (CO):

CO1	To understand digital logic principles, IC gates, and interfacing in practical circuits.
CO2	To apply logic representation, simplification, and digital circuit components for problem-solving.
CO3	To understand flip-flops, counters, and memory elements for digital circuit design.
CO4	To analyse digital-to-analog and analog-to-digital converters in signal processing systems.
CO5	To understand memory organization, types, and programmable devices in digital systems.

MAPPING OF COs AND POs

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO 1**	**PSO 2**	**PSO 3**
CO1	3.00	0.00	1.00	0.00	1.00	2.00	0.00	0.00	0.00	0.00	2.00	1.00	3.00	0.00	0.00
CO2	1.00	3.00	3.00	2.00	1.00	1.00	1.00	0.00	0.00	2.00	2.00	2.00	2.00	2.00	2.00
CO3	3.00	1.00	3.00	1.00	2.00	1.00	0.00	1.00	3.00	0.00	2.00	2.00	2.00	2.00	3.00
CO4	1.00	2.00	1.00	1.00	1.00	0.00	1.00	1.00	1.00	1.00	2.00	1.00	0.00	0.00	2.00
CO5	1.00	1.00	2.00	1.00	1.00	1.00	1.00	0.00	1.00	1.00	2.00	1.00	2.00	0.00	2.00

Correlation level: 1- slight (Low) 2- moderate (Medium) 3-substantial (High)

CO	Course outcomes	POs/PSOs	CL	Classroom session
CO1	To understand digital logic principles, IC gates, and interfacing in practical circuits.	PO 1, 3,5,6,11,12 PSO 1	U	7
CO2	To apply logic representation, simplification, and digital circuit components for problem-solving.	PO 1, 2, 3,4,5,6,11,12 PSO 1,2,3	Ap	7
CO3	To understand flip-flops, counters, and memory elements for digital circuit design.	PO 1,2,3,4,5,6,8,9, 11, 12 PSO 1,2,3	U	7
CO4	To analyse digital-to-analog and analog-to-digital converters in signal processing systems.	PO 1,2,3,4,5,7,8,9,10,11,12	An	7
CO5	To understand memory organization, types, and programmable devices in digital systems.	PO 1,2 3,4, 5,6,7,9,10,11, 12 PSO 1,3	U	7
				35

Cognitive Level (CL):
R-Remember, U-Understand, Ap- Apply, An-Analyse, E-Evaluate and C-Create

PO'S / PSO'S ADDRESSED BY COS & MAPPING STRENGTH WITH COURSE

PO/PSO	CO	No. of Sessions	% of session	Mapping Strength
PO1	CO 1,2,3,4,5	35	100	3
PO2	CO 2,3,4,5	28	80	3
PO3	CO 1,2,3,4,5	35	100	3
PO4	CO 2,3,4,5	28	80	3
PO5	CO 1,2,3,4,5	35	100	3
PO6	CO 1,2,3,5	28	100	3
PO7	CO 2,4,5	21	60	2
PO8	CO 3,4	14	40	2
PO9	CO 3,4,5	21	60	2
PO10	CO 2,4,5	21	60	2
PO11	CO 1,2,3,4,5	35	100	3
PO12	CO 1,2,3,4,5	35	100	3
PSO1	CO 1,2,3,5	28	80	3
PSO2	CO 2,3	14	40	2
PSO3	CO 2,3,4,5	28	80	3

S. No.	Percentage of Session	Mapping Strength
1	> 70	3
2	30 - 70	2
3	< 30	1

COURSE – PO/PSO MAPPING

DE	PO												PSO		
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**1**	**2**	**3**
Mapping Strength	3	3	3	3	3	3	2	2	2	2	3	3	3	2	3

SYLLABUS:

Topics	Number of Lectures	Weightage (%)
Fundamentals of Digital Systems and logic families Digital signals, digital circuits, AND, OR, NOT, NAND, NOR and Exclusive-OR operations, Boolean algebra, examples of IC gates, number systems-binary, signed binary, octal hexadecimal number, binary arithmetic, one's and two's complements arithmetic, codes, error detecting and correcting codes, characteristics of digital lCs, digital logic families, TTL, Schottky TTL and CMOS logic, interfacing CMOS and TTL, Tri-state logic.	7	20
Combinational Digital Circuits Standard representation for logic functions, K-map representation, simplification of logic functionsusing K-map, minimization of logical functions. Don't care conditions, Multiplexer, De-Multiplexer/Decoders, Adders, Subtractors, BCD arithmetic, carry look ahead adder, serial adder,ALU, elementary ALU design, popular MSI chips, digital comparator, parity checker/generator, codeconverters, priority encoders, decoders/drivers for display devices, Q-M method of function realization.	7	20
Sequential circuits and systems A 1-bit memory, the circuit properties of Bistable latch, the clocked SR flip flop, J- K-T and Dtypesflipflops,applicationsofflipflops,shiftregisters,applicationsofshiftregisters,serial to parallelconverter, parallel to serial converter, ring counter, sequence generator, ripple(Asynchronous) counters, synchronous counters, counters design using flip flops, special counter IC's, asynchronous sequential counters, applications of counters.	7	20
A/D and D/A Converters Digital to analog converters: weighted resistor/converter, R-2R Ladder D/A converter, specificationsfor D/A converters, examples of D/A converter lCs, sample and hold circuit, analog to digital converters: quantization and encoding, parallel comparator A/Dconverter, successive approximationA/D converter, counting A/D converter, dual slope A/D converter, A/D converter using voltagetofrequencyandvoltagetotimeconversion,specificationsofA/Dconverters, example of A/D converter ICs	7	20
Semiconductor memories and Programmable logic devices. Memory organization and operation, expanding memory size, classification and characteristics of memories, sequential memory, read only memory (ROM), read and write memory(RAM), content addressable memory (CAM), charge de coupled device memory (CCD), commonly used memory chips, ROM as a PLD, Programmable logic array, Programmable array logic, complex Programmable logic devices (CPLDS), Field Programmable Gate Array (FPGA).	7	20
Total``	**35**	100%

TIME TABLE

B.Tech. 4th Semester, Electrical Engineering Department

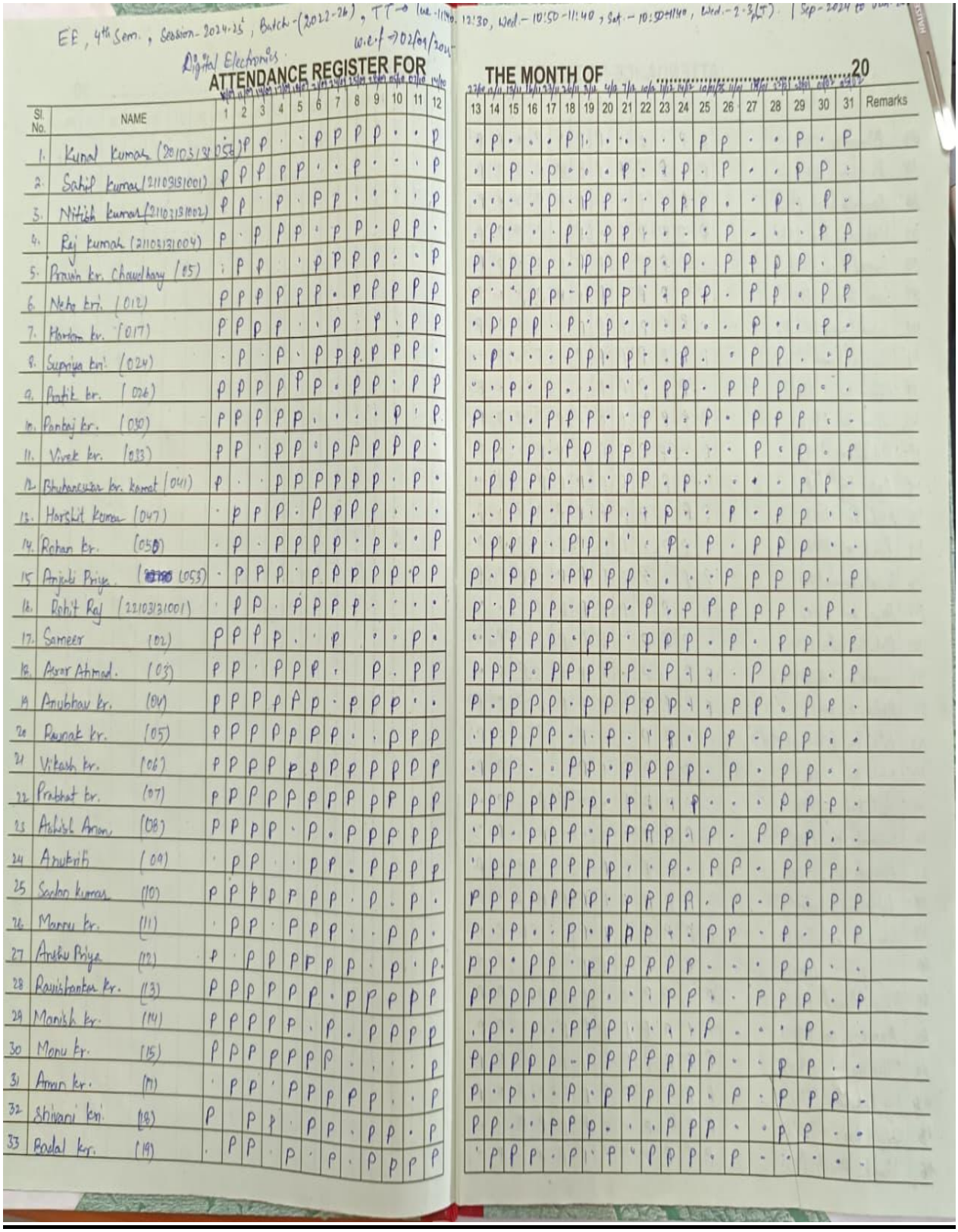
ROOM NO. 208, wef- 02/09/2024, Batch-2022-26						
	10:00 - 10:50	**10:50 - 11:40**	**11:40 - 12:30**	**12:30 – 1: 20**	**1:20 – 2:00**	**2-4:30pm**
MON					**R**	
TUES			DE		**E**	DE Lab
WED		DE			**C**	DE (T)
THUR						DE Lab
FRI					**E**	
SAT		DE			**S** **S**	
Faculty Name : Tabish Shanu						

List of Students-

S.N	Registration No.	Student Name
1	21103131001	SAHIL KUMAR
2	21103131002	NITISH KUMAR
3	21103131004	RAJ KUMAR
4	21103131012	NEHA KUMARI
5	21103131017	HARIOM KUMAR
6	21103131024	SUPRIYA KUMARI
7	21103131026	PRATIK KUMAR
8	21103131030	PANKAJ KUAMR
9	21103131033	VIVEK KUMAR
10	21103131047	HARSHIT KUMAR
11	21103131053	ANJALI PRIYA
12	22103131001	ROHIT RAJ
13	22103131002	SAMEER
14	22103131003	ASRAR AHMAD
15	22103131004	ANUBHAV KUMAR
16	22103131006	VIKASH KUMAR
17	22103131007	PRABHAT KUMAR
18	22103131008	ASHISH AMAN
19	22103131009	ANUKRITI
20	22103131010	SADAN KUMAR
21	22103131011	MANNU KUMAR
22	22103131012	ANSHU PRIYA
23	22103131013	RAVISHANKAR KUMAR
24	22103131014	MANISH KUMAR
25	22103131015	MONU KUMAR
26	22103131017	AMAN KUMAR
27	22103131018	SHIVANI KUMARI
28	22103131019	BADAL KUMAR
29	22103131020	ABHINAY KUMAR
30	22103131023	ANUSHKA SINGH
31	22103131025	UTKARSH JHA
32	22103131027	KOMAL KUMAR
33	22103131029	SONI PRIYA
34	22103131030	GHANSHYAM KUMAR

35	22103131032	SUMAN KUMAR
36	22103131033	SHIVAM KUMAR
37	22103131034	VIJAY KUMAR
38	22103131035	ASHISH KUMAR
39	22103131036	ANKIT RAJ PRINCE
40	22103131037	NISHA KUMARI
41	22103131038	ROHIT KUMAR
42	22103131039	SAKSHI SUMAN
43	22103131040	ARYAN KUMAR
44	22103131042	PINTU KUMAR YADAV
45	22103131043	PARMESHWARI BHARTI
46	22103131044	ABHAY KUMAR
47	22103131911	SILKI KUMARI
48	23103131901	NEHA KUMARI
49	23103131902	YASH RAJ
50	23103131903	SATIMALA KUMARI
51	23103131904	AVINASH KUMAR
52	23103131905	PRIYANSHU BHARTI
53	23103131906	SHIVANI KUMARI
54	23103131907	VIJAY KUMAR
55	23103131908	KHUSHI ANAND
56	23103131909	ANUPRIYA KUMARI
57	23103131910	MUSKAN KUMARI
58	23103131911	RAJLAKSHMI
59	23103131912	SHWETA KUMARI
60	23103131913	YAMIKA BHARTI
61	23103131914	RITESH KUMAR
62	23103131915	RAMESH KUMAR SAH
63	23103131916	KRISHAN KUMAR
64	23103131917	KUNDAN KUMAR YADAV
65	23103131918	KANHAIYA KUMAR
66	23103131919	VIKAS KUMAR RAM

ATTENDANCE



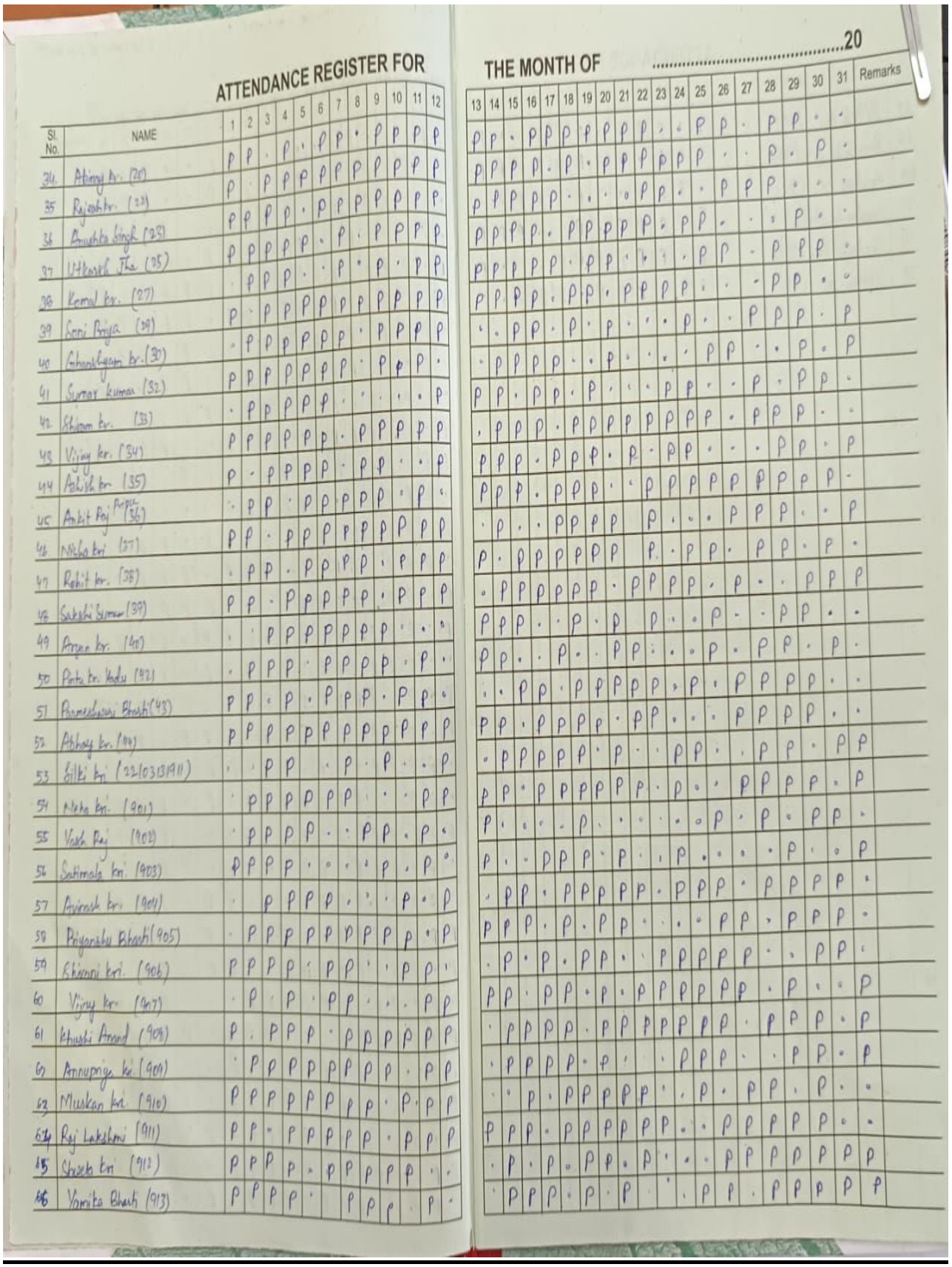
EE, 4th Sem., Session- 2024-25, Batch-(2022-26), TT → Tue-11:40, 12:30, Wed.- 10:50-11:40, Sat.- 10:50-11:40, Wed.- 2-3 (T) | Sep-2024 to Dec-2024

w.e.f → 02/09/2024

Digital Electronics

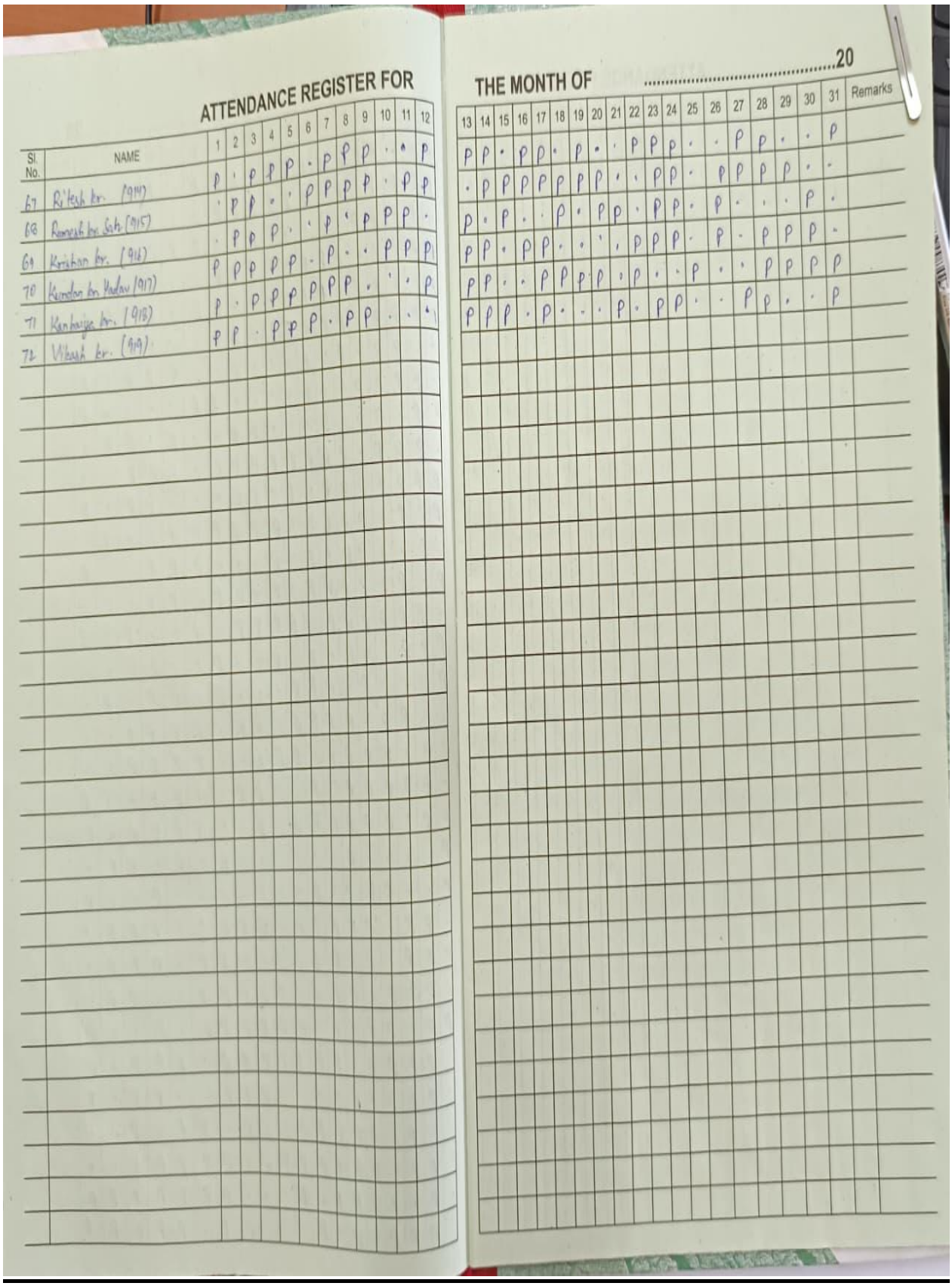
ATTENDANCE REGISTER FOR THE MONTH OF 20

Sl. No.	NAME	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	Remarks
1.	Kunal Kumar (21103131058)	P	P	P	·	·	P	P	P	P	·	·	P	·	P	·	·	·	P	P	·	·	·	·	·	P	P	·	·	P	·	P	
2.	Sahil Kumar (21103131001)	P	P	P	P	P	·	·	P	·	·	·	P	·	·	P	·	P	·	·	P	·	P	·	P	·	·	P	P	·			
3.	Nitish Kumar (21103131002)	P	P	·	P	·	P	P	·	·	·	·	P	·	·	·	P	·	P	P	·	·	P	P	P	·	·	P	·	P			
4.	Raj Kumar (21103131004)	P	·	P	P	P	·	P	P	·	P	P	·	·	P	·	·	·	P	·	P	P	·	·	·	P	·	·	·	P	P		
5.	Pravin kr. Chaudhary (05)	·	P	P	·	·	P	P	P	P	·	·	P	P	·	P	·	P	P	P	·	P	·	P	P	P	P	·	P				
6.	Neha kri. (012)	P	P	P	P	P	P	·	P	P	P	P	P	P	·	·	P	P	·	P	P	·	P	P	P	·	P	P	·	P	P		
7.	Harsh kr. (017)	P	P	P	P	·	·	P	·	P	·	P	P	·	P	·	·	·	P	·	·	·	·	·	P	·	·	P	·	P			
8.	Supriya kri. (024)	·	P	·	P	·	P	P	P	P	P	P	·	·	P	P	·	·	P	P	·	·	·	·	·	P	·	·	P	·			
9.	Ankit kr. (026)	P	P	P	P	P	P	·	P	P	·	P	P	·	·	P	P	·	P	P	·	P	·	P	P	P	P	·	P				
10.	Pankaj kr. (030)	P	P	P	P	P	·	·	·	·	P	·	P	·	P	·	·	·	P	·	P	·	P	P	P	·	·	P	·				
11.	Vivek kr. (033)	P	P	·	P	P	·	P	P	P	P	P	·	·	·	P	·	P	·	P	·	P	·	P	·	P	·	P	·				
12.	Bhubaneswar kr. Kamat (041)	P	·	·	P	P	P	P	P	P	·	P	·	·	P	P	P	·	P	P	P	·	P	·	P	P	P	·	·				
13.	Harshit Kumar (047)	·	P	P	P	·	P	P	P	P	·	·	·	·	·	P	P	·	P	·	P	·	P	·	P	P	P	·	·				
14.	Rohan kr. (050)	·	P	·	P	P	P	P	·	P	·	·	P	·	P	·	P	P	·	P	·	P	·	P	P	P	·	·					
15.	Anjali Priya. (053)	·	P	P	P	·	P	P	P	P	P	P	P	P	·	P	P	·	P	P	P	P	P	·	·	·	P	P	P	P	·	P	
16.	Rohit Raj (22103131001)	·	P	P	·	P	P	P	P	·	·	·	·	P	·	P	P	P	·	P	·	P	P	P	P	P	·	P	·				
17.	Sameer (02)	P	P	P	P	·	·	P	·	·	·	P	·	·	·	P	P	P	·	P	·	P	P	P	·	P	·	P	P	·	P		
18.	Asrar Ahmad. (03)	P	P	·	P	P	P	·	·	P	·	P	P	P	P	·	P	P	P	·	P	·	·	P	P	P	·	P					
19.	Anubhav kr. (04)	P	P	P	P	P	P	·	P	P	P	·	·	P	·	P	P	P	·	P	P	P	P	P	·	P	P	·	P	P	·		
20.	Ramak kr. (05)	P	P	P	P	P	P	P	·	·	P	P	P	·	P	P	P	P	·	·	P	·	P	P	·	P	P	·	·				
21.	Vikash kr. (06)	P	P	P	P	P	P	P	P	P	P	P	P	·	P	P	·	·	P	P	·	P	P	P	P	·	P	·	P	P	·		
22.	Prabhat kr. (07)	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	·	P	·	·	·	·	P	P	P	·				
23.	Ashish Aman. (08)	P	P	P	P	·	P	·	P	P	P	P	P	·	P	·	P	P	P	·	P	P	P	·	P	P	P	·	·				
24.	Anukriti (09)	·	P	P	·	·	P	P	·	P	P	P	P	·	P	P	P	P	P	P	·	P	·	P	P	P	·	P	·				
25.	Sachin kumar (10)	P	P	P	P	P	P	P	·	P	·	P	·	P	P	P	P	P	P	P	P	·	P	P	·	P	P	P	·				
26.	Manoj kr. (11)	·	P	P	·	P	P	P	·	·	P	P	·	P	·	P	·	P	·	P	·	P	P	·	P	·	P	P	·				
27.	Anshu Priya (12)	P	·	P	P	P	P	P	P	·	P	·	P	P	P	·	P	P	P	P	P	P	·	·	·	P	P	·	·				
28.	Ravishankar kr. (13)	P	P	P	P	P	P	·	P	P	P	P	P	P	P	P	P	P	P	P	·	·	P	P	·	P	P	P	·	P			
29.	Manish kr. (14)	P	P	P	P	P	·	P	·	P	P	P	P	·	P	·	P	·	P	P	P	·	·	·	P	·	·	P	·	·			
30.	Monu kr. (15)	P	P	P	P	P	P	P	·	·	·	·	P	P	·	P	·	P	P	P	P	P	·	·	P	P	·	·					
31.	Aman kr. (17)	·	P	P	·	P	P	P	P	P	·	·	P	P	·	P	·	P	P	P	P	P	·	P	·	P	P	P	·				
32.	Shivani kri. (18)	P	·	P	P	·	P	P	·	P	P	·	P	P	·	·	P	P	·	·	P	P	P	·	·	P	P	·	·				
33.	Badal kr. (19)	·	P	P	·	P	·	P	·	P	P	P	P	·	P	P	P	·	P	·	P	P	P	·	P	·	·	·	·				



ATTENDANCE REGISTER FOR THE MONTH OF 20

Sl. No.	NAME	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	Remarks
34	Abhay kr. (20)	P	P	.	P	.	P	P	.	P	P	P	P	P	P	.	P	P	P	P	P	P	P	.	.	P	P	.	P	P	.	.	
35	Rajesh kr. (23)	P	.	P	P	P	P	P	P	P	P	P	P	P	P	P	P	.	.	P	.	P	P	.	P	P	.	P	P	P	.	.	
36	Anushka Singh (28)	P	P	P	P	.	P	P	P	P	P	P	P	P	P	P	P	.	.	.	P	P	.	.	P	P	P	.	.	P	.	.	
37	Utkarsh Jha (25)	P	P	P	P	P	.	P	.	P	P	P	P	P	P	P	P	.	P	P	P	P	.	P	P	.	P	P	P	.	.	.	
38	Kamal kr. (27)	.	P	P	P	.	.	P	.	P	.	P	P	P	P	.	P	P	P	.	P	P	P	.	.	.	P	P	.	.	P	.	
39	Soni Priya (29)	P	.	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	.	P	P	P	P	P	P	P	P	P	.	P	
40	Gobardhan kr. (30)	.	P	P	P	P	P	P	.	P	P	P	P	.	.	P	P	.	P	.	.	.	P	.	.	P	P	.	.	P	.	P	
41	Sumar kumar (32)	P	P	P	P	P	P	P	.	P	P	P	.	.	P	P	P	P	.	P	.	.	.	P	P	.	.	P	.	P	P	.	
42	Shivam kr. (33)	.	P	P	P	P	P	.	.	.	.	P	.	P	P	P	P	.	P	P	P	P	P	P	P	.	P	P	P	.	.		
43	Vijay kr. (34)	P	P	P	P	P	P	.	P	P	P	P	P	P	P	P	.	P	P	P	.	P	P	P	P	.	.	P	P	.	P		
44	Ashish kr. (35)	P	.	P	P	P	P	.	P	P	.	.	P	P	P	P	.	P	P	.	P	P	.	.	.	P	P	.	P				
45	Ankit Raj Pipra (36)	.	P	P	.	P	P	P	P	P	.	P	.	P	.	.	P	P	P	P	.	P	P	P	P	P	P	P	P	P	-		
46	Nisha kri (37)	P	P	.	P	P	P	P	P	P	P	P	P	.	P	.	.	P	P	P	P	.	.	P	P	P	.	.	P				
47	Rohit kr. (38)	.	P	P	.	P	P	P	P	.	P	P	P	P	.	P	P	P	P	P	P	.	P	P	.	P	P	.	P	.			
48	Sakshi Sumar (39)	P	P	.	P	P	P	P	P	.	P	P	P	.	P	P	P	P	P	P	P	.	P	P	P	.	.	P	P	P			
49	Aryan kr. (40)	.	.	P	P	P	P	P	P	P	.	.	.	P	P	P	.	P	P	P	.	.	P	-	-	P	P	.	.				
50	Pinta kr. Yadav (42)	.	P	P	P	.	P	P	P	P	.	P	.	P	P	.	P	.	.	P	P	P	P	.	.	P	P	P	.	P			
51	Parmeshwari Bharti (43)	P	P	.	P	.	P	P	P	.	P	P	.	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P			
52	Abhay kr. (44)	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P			
53	Silki kri (22/03/2011)	.	.	P	P	.	.	P	.	P	.	.	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P			
54	Nisha kri. (901)	.	P	P	P	P	P	P	.	.	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P			
55	Vivek Raj (902)	.	P	P	P	P	.	.	P	P	.	P	.	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P			
56	Satimala kri. (903)	P	P	P	P	.	.	.	.	P	.	P	.	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P			
57	Avinash kr. (904)	.	.	P	P	P	P	.	.	.	P	.	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P			
58	Priyanshu Bharti (905)	.	P	P	P	P	P	P	P	P	P	.	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P			
59	Shivani kri. (906)	P	P	P	P	.	P	P	.	.	P	P	.	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P			
60	Vijay kr. (907)	.	P	.	P	.	P	P	.	.	.	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P			
61	Khushi Anand (908)	P	.	P	P	P	.	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P			
62	Annupriya kr. (909)	.	P	P	P	P	P	P	P	P	.	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P			
63	Muskan kri. (910)	P	P	P	P	P	P	P	P	.	P	.	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P			
64	Raj Lakshmi (911)	P	P	.	P	P	P	P	P	.	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P			
65	Shweta kri (912)	P	P	P	P	.	P	P	P	P	P	.	.	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P			
66	Vanita Bharti (913)	P	P	P	P	.		P	P	P	.	P	.	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P			



ATTENDANCE REGISTER FOR THE MONTH OF 20

Sl. No.	NAME	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	Remarks
67	Ritesh kr. (914)	P	·	P	P	P	·	P	P	P	·	·	P	P	P	·	P	P	·	P	·	·	P	P	P	·	·	P	P	·	·	P	
68	Ramesh kr. Sah (915)	·	P	P	·	·	P	P	P	P	·	P	P	·	P	P	P	P	P	P	P	·	·	P	P	·	P	P	P	P	·	·	
69	Krishan kr. (916)	·	P	P	P	·	·	P	·	P	P	P	·	P	·	P	·	P	·	P	P	·	P	P	·	P	·	·	·	P	·		
70	Kundan kr. Yadav (917)	P	P	P	P	P	·	P	·	·	P	P	P	P	P	·	P	P	·	·	,	P	P	P	·	P	·	P	P	P	P		
71	Kanhaiya kr. (918)	P	·	P	P	P	P	P	·	·	·	·	P	P	·	·	P	P	P	·	P	·	·	P	·	·	P	P	P	P	P		
72	Vikash kr. (919)	P	P	·	P	P	P	·	P	P	·	·	·	P	P	P	·	P	·	·	P	·	P	P	·	·	P	P	·	·	P		

Lecture Plan

Text Books:

TB1: R. P. Jain, "Modern Digital Electronics", McGraw Hill Education, 2009.
TB2: M. M. Mano, "Digital logic and Computer design", Pearson Education India, 2016.
Reference Books:
RB2: A. Kumar, "Fundamentals of Digital Circuits", Prentice Hall India, 2016.

Lecture No.	Topics	Text books/Reference books
1-2	Digital signals, digital circuits, AND, OR, NOT, NAND, NOR and Exclusive-OR operations	TB1
3-4	Boolean algebra, examples of IC gates, number systems-binary, signed binary, octal hexadecimal number, binary arithmetic,	TB1 , TB2
5	one's and two's complements arithmetic, codes, error detecting and correcting codes, characteristics of digital lCs,	TB1, RB1
6-7	digital logic families, TTL, Schottky TTL and CMOS logic, interfacing CMOS and TTL, Tri-state logic.	TB1
8-9	Standard representation for logic functions, K-map representation,	TB1 , TB2
10-11	simplification of logic functionsusing K-map, minimization of logical functions. Don't care conditions,	TB1 , RB1
12	Multiplexer, De-Multiplexer/Decoders, Adders, Subtractors, BCD arithmetic, carry look ahead adder, serial adder,ALU, elementary ALU design,	TB1 , TB2
13-14	popular MSI chips, digital comparator, parity checker/generator, codeconverters, priority encoders, decoders/drivers for display devices, Q-M method of function realization.	TB1 , RB1
15-17	A 1-bit memory, the circuit properties of Bistable latch, the clocked SR flip flop, J- K-T	TB1 , TB2
18-19	Dtypesflipflops,applicationsofflipflops,shiftregisters,applicationsofshiftregisters,serial to parallelconverter,	TB1
20	parallel to serial converter, ring counter, sequence generator, ripple(Asynchronous)	TB1 , RB1

	counters,	
21	synchronous counters, counters design using flip flops, special counter IC's, asynchronous sequential counters, applications of counters.	TB1 , TB2
22-23	Digital to analog converters: weighted resistor/converter, R-2R Ladder D/A converter,	TB1 , RB1
24-26	specificationsfor D/A converters, examples of D/A converter lCs, sample and hold circuit, analog to digital converters: quantization and encoding, parallel comparator A/Dconverter, successive approximationA/D converter,	TB2
27-28	counting A/D converter, dual slope A/D converter, A/D converter using voltagetofrequencyandvoltagetotimeconversion,specificationsofA/Dconverters, example of A/D converter ICs	TB2
29-31	Memory organization and operation, expanding memory size, classification and characteristics of memories, sequential memory, read only memory (ROM), read and write memory(RAM),	RB1
32	Content addressable memory (CAM), charge de coupled device memory (CCD),	TB1
33-34	commonly used memory chips, ROM as a PLD, Programmable logic array, Programmable array logic	RB1
35	complex Programmable logic devices (CPLDS), Field Programmable Gate Array (FPGA).	TB1 , TB2

Topics	**Lecture Covered**	**CO covered**
Digital signals, digital circuits	**1**	**CO1**
AND, OR, NOT, NAND, NOR and Exclusive-OR operations	**2**	**CO1**
Boolean algebra, examples of IC gates	**3**	**CO1**
number systems-binary, signed binary, octal hexadecimal number, binary arithmetic	**4**	**CO1**
one's and two's complements arithmetic, codes, error detecting and correcting codes, characteristics of digital lCs,	**5**	**CO1**
digital logic families, TTL, Schottky TTL and CMOS logic,	**6**	**CO1**
interfacing CMOS and TTL, Tri-state logic.	**7**	**CO1**
Standard representation for logic functions	**8**	**CO2**
K-map representation,	**9**	**CO2**
simplification of logic functionsusing	**10**	**CO2**
K-map, minimization of logical functions. Don't care conditions,	**11**	**CO2**

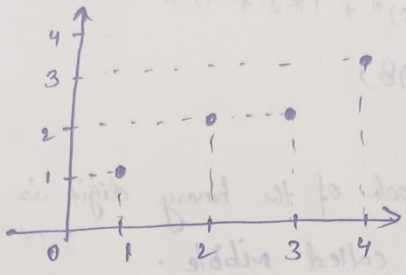
Multiplexer, De- Multiplexer/Decoders, Adders, Subtractors, BCD arithmetic, carry look ahead adder, serial adder,ALU, elementary ALU design,	**12**	**CO2**
popular MSI chips, digital comparator, parity checker/generator,	**13**	**CO2**
codeconverters, priority encoders, decoders/drivers for display devices, Q-M method of function realization.	**14**	**CO2**
A 1-bit memory, the circuit properties of Bistable latch,	**15**	**CO3**
the circuit properties of Bistable latch,	**16**	**CO3**
the clocked SR flip flop, J- K-T	**17**	**CO3**
Dt ypes flipflops, applications of flipflops	**18**	**CO3**
shiftregisters, applications of shiftregisters	**19**	**CO3**
serial to parallel converter,	**20**	**CO3**
synchronous counters, counters design using flip flops, special counter IC's, asynchronous sequential counters, applications of counters.	**21**	**CO3**
Digital to analog converters:	**22**	**CO4**
weighted resistor/converter, R-2R Ladder D/A converter,	**23**	**CO4**
specificationsfor D/A converters, examples of D/A converter lCs, sample and hold circuit,	**24**	**CO4**
analog to digital converters: quantization and encoding	**25**	**CO4**
parallel comparator A/Dconverter, successive approximationA/D converter,	**26**	**CO4**
counting A/D converter, dual slope A/D converter, A/D converter using	**27**	**CO4**
voltagetofrequencyandvoltagetotimeconversion,specificationsofA/Dconverters, example of A/D converter ICs	**28**	**CO4**
Memory organization and operation, expanding memory size,	**29**	**CO5**
classification and characteristics of memories, sequential memory	**30**	**CO5**
read only memory (ROM), read and write memory(RAM),	**31**	**CO5**
Content addressable memory (CAM), charge de coupled device memory (CCD)	**32**	**CO5**
commonly used memory chips, ROM as a PLD,	**33**	**CO5**
Programmable logic array, Programmable array logic	**34**	**CO5**
complex Programmable logic devices (CPLDS), Field Programmable Gate Array (FPGA).	**35**	**CO5**

Digital Electronics

(1)

→ Digital signal are the signal that represents data in terms of sequence of discrete values.

→ It represents only finite values a number of discrete values.



Digital Circuit → A digital circuit is designed by using a number of logic gates on a single integrated circuit - IC. The input to any digital circuit is in binary form '0' or '1'. These circuits can be represented in 2-ways either combinational or a sequential way.

Number System :-

Decimal number system - commonly used.
Binary, octal, hexadecimal etc. systems, → others.

Decimal → It is having 10 digits with base 10 system.

Binary ⇒ It is having two digits (0 or 1) with base two system.
⇒ The position of 0 & 1 in a binary number indicates its 'weight' within the number.

$(198)_{10} = 8\times10^0 + 9\times10^1 + 1\times10^2$ → decimal number.

Positional weights.

$(198)_{10} = (11000110)_2$

$= 0\times2^0 + 1\times2^1 + 1\times2^2 + 0\times2^3 + 0\times2^4 + 0\times2^5 + 1\times2^6 + 1\times2^7$

$= (198)$

→ In binary system each of the binary digit is called a bit.

→ Group of 4-bits is called nibble.

→ Group of 8-bits is called byte.

→ The highest decimal no. that can be represented by n-bits binary number is $2^n - 1$.

eg ⇒ max. decimal no. that can be represented with 8 bit binary is $2^8 - 1 = 255$.

Decimal to binary conversion →.

Eg. 53.625 → 53 + 0.625

Integer, fraction.

2 | 53	1	← LSB
2 | 26	0	
2 | 13	1	
2 | 12	0	
2 | 6	0	
2 | 3	1	
	1	← MSB

110

2 | 53	
2 | 26	1
2 | 13	0
2 | 6	1
2 | 3	0
2 | 1	1

Decimal to Binary ⇒.

(2)

⇒ 53.625

Integer:

2 | 53	1	→ LSB
2 | 26	0	
2 | 13	1	
2 | 6	0	
2 | 3	1	
1		MSB

(110101)

Fraction:

Generated Integers.

0.625 × 2 = 1.25 → 1 → MSB

0.25 × 2 = 0.50 → 0

0.50 × 2 = 1.00 → 1

00 × 2 = 0.00 → 0 → LSB

(101)

further multiplying factor is not possible as the product is zero.

$(53.625)_{10} = (110101.101)_2$.

Ans.

Q). $(47.8125)_{10}$ ⟶ $(101111.1101)_2$

Eg:. Convert Binary to decimal ⇒. $(101.1101)_2$

$101 \Rightarrow 1\times2^0 + 0\times2^1 + 1\times2^2$

$\Rightarrow 1+0+4 = 5$

$0.1101 \Rightarrow 1\times2^{-1} + 1\times2^{-2} + 0\times2^{-3} + 1\times2^{-4}$.

$\Rightarrow 0.5 + 0.25 + 0 + 0.0625$

$\Rightarrow 0.8125$.

Ans ⇒ $(5.8125)_{10}$ Ans.

Q) $(1101.0011)_2$ ⟶ Decimal ⇒. $(13.1875)_{10}$. Ans.

$1101 \Rightarrow 1+0+4+8 \Rightarrow 13$

$0.0011 \Rightarrow 0+0+2^{-3}+2^{-4}$

$\Rightarrow 0.125 + 0.0625$

⇒ Octal Numbers ⇒ It uses digits ⇒ 0, 1, 2, 3, 4, 5, 6, 7

Base ⇒ 8.

Eg: Convert $(444.456)_{10}$ ⇒ Octal ?

Integer:

8 | 444 — 4 → LSB
8 | 55 — 7
6 → MSB

(674)

Fraction:

Generated digits

$0.456 \times 8 = 3.648$ — 3 MSB
$0.648 \times 8 = 5.184$ — 5
$0.184 \times 8 = 1.472$ — 1
$0.472 \times 8 = 3.776$ — 3
$0.776 \times 8 = 6.208$ — 6 LSB

Process is terminated when significant digits are obtained.

(0.35136)

$(674.35136)_8$.

Q) Convert octal to decimal ⇒.

a) $(237)_8 \rightarrow (159)_{10}$

$7 \times 8^0 + 3 \times 8^1 + 2 \times 8^2$

$\Rightarrow (159)_{10}$

b) $(120)_8 \rightarrow (80)_{10}$.

Q) Convert octal to binary ⇒

$(376)_8 \Rightarrow$ 3 (011) 7 (111) 6 (110) $\Rightarrow (011\,111\,110)_2$.

Q) Binary to octal ⇒ $(10011010101)_2$ ⇒ octal.

010 011 010 101

2 3 2 5

$\Rightarrow (2325)_8$.

(3)

Hexdecimal → 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F
(A = 10, B = 11, C = 12, D = 13, E = 14, F = 15)

Dec. → Hex.

Eg. $(115)_{10} \rightarrow (73)_{16}$

16 | 115
16 | 7
0

$(73)_{16}$

$(235)_{10} \rightarrow (EB)_{16}$.

16 | 235
16 | 14
0

11 (LSB)

MSB

14 → E
11 → B.
$(EB)_{16}$.

Hex. → Decimal.

$(2F3)_{16} = 3\times16^0 + F\times16^1 + 2\times16^2$.
$= (755)_{10}$.

Hex. → Binary. → $(2D5)_{16} = 2 \; D \; 5$
$0010 \; 1101 \; 0101$
$= (001011010101)_2$.

Bin. → Hex. $(111\,1011\,0101)_2 = 0111\;1011\;0101 = (7B5)_{16}$.
7 B 5

Hex → Octal. $(47)_{16} = (0100\;0111)_2$
$= (001\;000\;111) = (107)_8$.

Octal → Hex. $(32)_8 = (011\;010)$
$= (0001\;1010) = (1A)_{16}$.

Q) $(7.FD6)_{16} = (\;)_8$ Ans → $(7.7726)_8$.

$(0111.111110101110)_2 \Rightarrow (7.7726)_8$.

Q) $(7864)_{10} \rightarrow (\;)_{16}$, $(EBB)_{16}$.

25
19
05
419

⇒ 1's Compliment → Take complement of that number.

11001 —1's→ 00110.

0110 —1's→ 1001

⇒ Subtraction by 1's compliment →

Case I.

```
  1111
 -1010
 ------
  0101
```

Direct method.

1's complement method ⇒

```
  1111   (+)
  0101
 ------
 10100
```

1's complement.

Carry → +1

```
  0101   Ans.
 ------
```

Case II → Subtraction of a larger number →

```
  1000
 -1010.
 ------
 -0010
 ------
```

Direct method.

1's complement method →.

```
  1000
  0101
 ------
  1101
 ------
```

→ No carry, Ans will be 1's complement of 1101 i.e 0010 with opposite sign.

Ans → −0010.

2's complement method ⇒

2's complement ⇒ take 1's complement & then add 1 at LSB.

100110 —1's→ 011001

↓ 2's

011001
1
011010 → 2's comp.

Subtraction using 2's complement →

Case I

1111.
−1010.
0101 → Direct method

2's complement method ⇒.

Step1 → Take 2's complement of 1010 → 0101
1
0110

Step2 → Now add the no.'s.

1111 (+).
0110
10101
↓
carry.

Step3 → Carry is discarded.

Case II.

1000
−1010. (bigger no.)
0010.

1000
0110. → 2's complement.
No carry → 1110
↓
Take 2's complement of this no. & put −ve sign

1110 → 0001 (−0010) Ans.
1
0010

Codes. 8421 or BCD. (0 to 9)

Eg. 9642 → 9 6 4 2

↓ ↓ ↓ ↓

1001 0110 0100 0010

→ (10010110.01000010)$_{BCD}$.

⇒ Excess 3-code → Eg. 6 4 3

+3 +3 +3.

sum. → 9 7 6.

↓ ↓ ↓

Convert it to BCD. 1001 0111 0110

$[643]_{10}$ → Excess 3-code → (100101110110)

BCD ⇒ 0 to 9, After 9 i.e 10

↓ ↓

(0001 0000)$_{BCD}$.

(8421) code.

weighted positions.

Eg. 12 → In binary → $(1100.)_2$.

12 → In BCD. → (0001 0010)$_{BCD}$.

Decimal.	BCD.	Excess-3 code
0	0000	0011
1	0001	0100
2	0010	0101
3	0011	0110.
4	0100	0111
5	0101	1000
6	0110	1001
7	0111	1010.
8	1000	1011
9	1001	1100.

Excess 3 → Invalid group. → (0000, 0001, 0010, 1101, 1110, 1111)
(0) (1) (2) (13) (14) (15)

→ Gray Code → Binary to Gray

MSB
1 ⊕ 0 ⊕ 1 ⊕ 1 ⊕ 0 → Binary.
↓ EX-OR.
1 1 1 0 1 → Gray.

Gray to binary →

1 1 0 1 0 1 → Gray.
1 0 0 1 1 0. → Binary.

Q) Convert → $[10101101]_2$ → Gray ⇒ $[11111011]_{Gray}$

Q) Convert → $[1011]_{Gray}$ → Binary → $[1101]_2$

Hamming Code → Eg. 7 bit → $P_1 P_2 P_4$ ($2^0, 2^1, 2^2$) (Parity)
or
12 bit → $P_1 P_2 P_4 P_8$ ($2^0, 2^1, 2^2, 2^3$)

Data ⇒ 1101 → to be transmitted.

Format for 7 bit Hamming code -

①	②	③	④	⑤	⑥	⑦
P_1	P_2	D_3	P_4	D_5	D_6	D_7
LSB						MSB
0	0	1	0	1	1	

Data → 1

	P_4	P_2	P_1
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

For even parity.

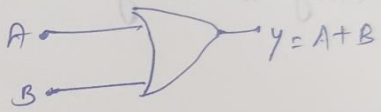
$P_1(1,3,5,7) = (P_1, 101) \Rightarrow P_1 = 0$ "

$P_2(2,3,6,7) = (P_2, 111) \Rightarrow P_2 = 1$ (for even parity)

$P_3(4,5,6,7) = (P_4, 011) \Rightarrow P_4 = 0$ "

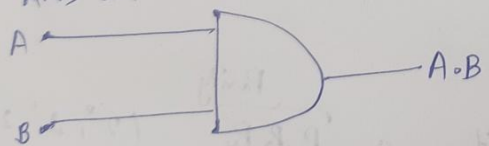
Logic Gates

① OR Gate



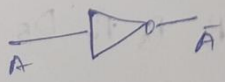
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

② AND Gate



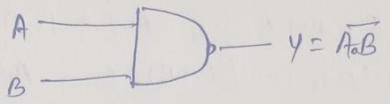
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

③ NOT Gate (Inverter Gate)



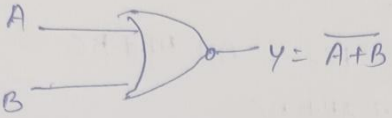
A	Y
0	1
1	0

NAND Gate :



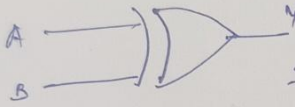
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

NOR Gate



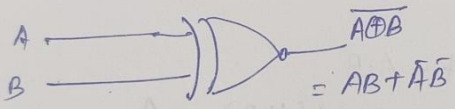
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Exclusive-OR (EX-OR) Gate



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

EX-NOR.



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Boolean Algebra → Boolean addition →

$0 + 0 = 0$
$0 + 1 = 1$
$1 + 0 = 1$
$1 + 1 = 1$

Boolean Multiplication :-

$0 \cdot 0 = 0$
$0 \cdot 1 = 0$
$1 \cdot 0 = 0$
$1 \cdot 1 = 1$

Boolean Laws.

$A + A = A$	$1 + A = 1$	$A + \bar{A} = 1$	$A \cdot 0 = 0$
$A \cdot A = A$	$1 \cdot A = A$	$A \cdot \bar{A} = 0$	$\bar{\bar{A}} = A$
		$A + 0 = A$	

Commutative property ⇒ $A+B=B+A$, $A\cdot B=B\cdot A$

Associative property ⇒ $A+(B+C)=(A+B)+C$, $A\cdot(B\cdot C)=(A\cdot B)\cdot C$

Distributive property ⇒ $A+BC=(A+B)(A+C)$

$$A+BC = A\cdot 1+BC$$
$$= A(1+B)+BC = A+AB+BC$$
$$= A(1+C)+AB+BC$$
$$= A+AC+AB+BC$$
$$= A\cdot A+AC+AB+BC = A(A+C)+B(A+C)$$
$$= (A+B)(A+C).$$

Absorption law :- $A+AB=A$

$$\Rightarrow A(1+B)=A.$$

Eg. → $A(A+B) = A\cdot A+A\cdot B$
$$= A+AB = A(1+B) = A$$

$(A+\bar{A}B)^{*}$ $= (A+\bar{A})(A+B) = \underline{A+B.}$

Eg. $A(\bar{A}+B) = AB$

Demorgan's law :-

$$\overline{AB} = \bar{A}+\bar{B}$$

$$\overline{A+B} = \bar{A}\cdot\bar{B}$$

Q^ws) Simplify the expressions –

(1) $A + A\cdot\bar{B} + \bar{A}\cdot B = A(1+\bar{B}) + \bar{A}\cdot B$

$= A\cdot 1 + \bar{A}\cdot B = (A+\bar{A})(A+B) = A+B.$

(2) Q. $\overline{\bar{A}B + C\bar{D}} = (\overline{\bar{A}B})\cdot(\overline{C\bar{D}})$

$= (\bar{\bar{A}}+\bar{B})\cdot(\bar{C}+\bar{\bar{D}}) = (A+\bar{B})(\bar{C}+D)$

(3) Simplify the exp. – ~~$\bar{A}\bar{B} + ABC + A(B+A\bar{B})$~~

$(A+B)(\bar{A}\bar{C}+C)(\overline{\bar{B}+AC}) = (A+B)+(\bar{A}\bar{C}+C)(\bar{\bar{B}}\cdot\overline{AC})$

$= (A+B)+(\bar{A}\bar{C}+C)(B\cdot\overline{AC})$.

$= (\underbrace{A\bar{A}\bar{C}}_{0} + AC + \bar{A}\bar{C}B + BC)\cdot[B\cdot(\bar{A}+\bar{B})]$

$= (AC + \bar{A}\bar{C}B + BC)[\bar{A}B + B\bar{B}]$

$= \bar{A}BC + \bar{A}\bar{B}C + \bar{A}BC = \bar{A}B(C+\bar{C}) = \bar{A}B\cdot 1$

(4) $Y = \bar{A}B + ABD + A\bar{B}C\bar{D} + BC$

$= B(\bar{A}+AD) + C(B+\bar{B}A\bar{D})$

$= B(\bar{A}+D) + C(B+A\bar{D})$

$= \bar{A}B + BD + BC + AC\bar{D}$

$= \bar{A}B + BD + BC(A+\bar{A}) + AC\bar{D}$

$= \bar{A}B + BD + ABC + \bar{A}BC + AC\bar{D}$

$= \bar{A}B(1+C) + BD + ABC + AC\bar{D}$

$= \bar{A}B + BD + AC\bar{D}$

$\{(\bar{A}+A)(\bar{A}+D) \Rightarrow \bar{A}+D.$

Simplify →

Q) $Y = ((AB) + \bar{A}\bar{B})(\bar{C}\bar{D} + CD) + \overline{\bar{A}\bar{C}}$

$Y = AB\bar{C}\bar{D} + ABCD + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A} + \bar{C}$

$= \bar{A}(1 + \bar{B}\bar{C}\bar{D} + \bar{B}CD) + \bar{C}(1 + AB\bar{D}) + ABCD$

$= \bar{A} + \bar{C} + ABCD.$

Q) $\overline{\bar{A}\bar{B}C + (\overline{A+B+C}) + \bar{A}\bar{B}\bar{C}D} = A + B$

Q) $Y = AB + A(B+C) + B(B+C)$

$= \cancel{AB + A(B+C)}$

$= AB + AB + AC + BB + BC$

$= AB + AC + B + BC = AB + AC + B(1+C)$

$= \cancel{AB} \; AB + AC + B.$

$= B(1+A) + AC = B + AC$

Characteristics of Digital IC's →

① Speed of operation - (Propagation delay) -

→ The speed of operation of an IC is expressed in terms of propagation delay.

→ Propagation delay is defined as the time taken for the output of a gate to change after the inputs have changed.

→ t_{PLH} → propagation delay in going from Low to High (0 to 1)

→ t_{PHL} → " " " High to low (1 to 0)

② Power dissipation → It is a measure of the power consumed by the logic gate when fully driven by all its input. (mW or nano Watt).

$$P_{dc(avg)} = V_{dc} \times I_{mean}$$

③ Fan-in → It is the no. of inputs connected to the gate without any degradation in the voltage levels.
This parameter defines the functional capabilities of a logic ckt.

④ Fan-out → Max. no. of similar logic gates that a gate can drive without voltage degradation.

⑤ Noise immunity → It is the maximum noise voltage that may appear at the input of a logic gate without changing logic state of the output.

⑥ Operating temperature → All IC's are temp. sensitive. The operating temp. of an IC ranges from 0 to +70°C for consumer & industrial application.

(7) Power supply requirement → The amount of power & supply voltage required by an IC are the main parameters to be taken in consideration while choosing a proper power supply.

Logic families →

① Transistor – Transistor logic (TTL or T^2L).

→ It has the fastest switching speed when compared to other logic families that utilize saturated transistors.

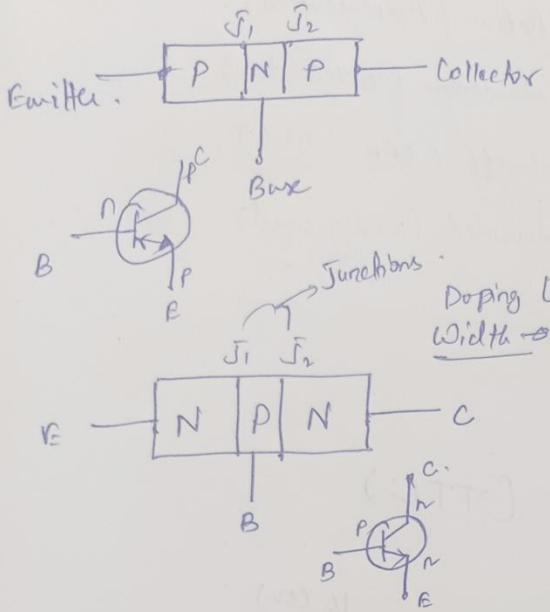
Typical Characteristics →

Supply voltage ⇒ 5V

Logical 0 o/p voltage	→ 0 to 0.4V.
" 1 " "	→ 2.4 to 5V
Logical 0 i/p "	→ 0 to 0.8V.
" 1 " "	→ 2V to 5V.
Noise immunity	0.4V.

→ TTL basic ckt is NAND gate.

Bipolar Junction Transistor (BJT).



Bipolar → both holes & e^{-s} are resp responsible for current conduction.

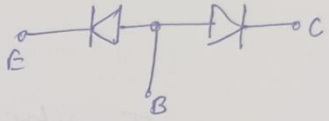
E ⇒ heavily doped, Base = lightly doped

Collector → moderately doped.

Doping level → E > C > B

Width → Base region is thin & collector is wider than emitter & base.

C > E > B.



Different regions of operation →

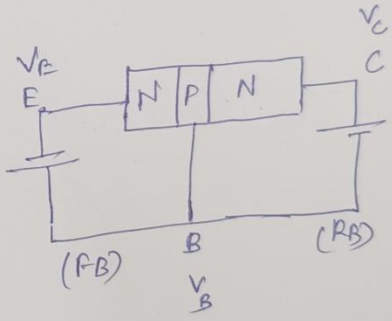
① Active region :-

J_1 – Emitter-base jn. is Forward biased.

J_2 – Base-collector jn is R.B

$V_B > V_E$

$V_C > V_B$.



② Cut-off region → E-B (J_1) jn is R.B & C-B (J_2) jn is R.B.

$V_E > V_B$, $V_C > V_B$.

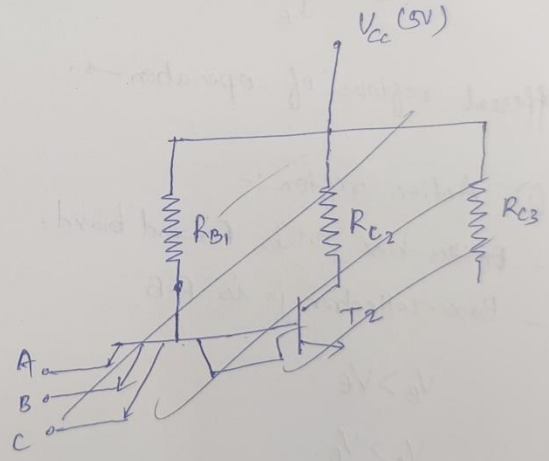
③ Saturation region → B-E (J_1) → F.B, B-C (J_2) jn is F.B

$V_B > V_E$, $V_B > V_C$.

(Emitter base J^n) J_1	(Collector-base J^n) J_2	Region.
(1) F.B	R.B	Active (Amplification).
(2) F.B	F.B	Saturation (ON-switch).
(3) R.B	R.B	Cut-off (OFF-switch).
(4) R.B	F.B	Inverted (rarely used)

Transistor – Transistor logic → (TTL)
(It is basically a NAND gate)

Circuit diagram:-



TTL

It is basically a NAND gate →

Logic 0 = 0.2V ($V_{CE\,sat}$).

logic 1 = 5V.

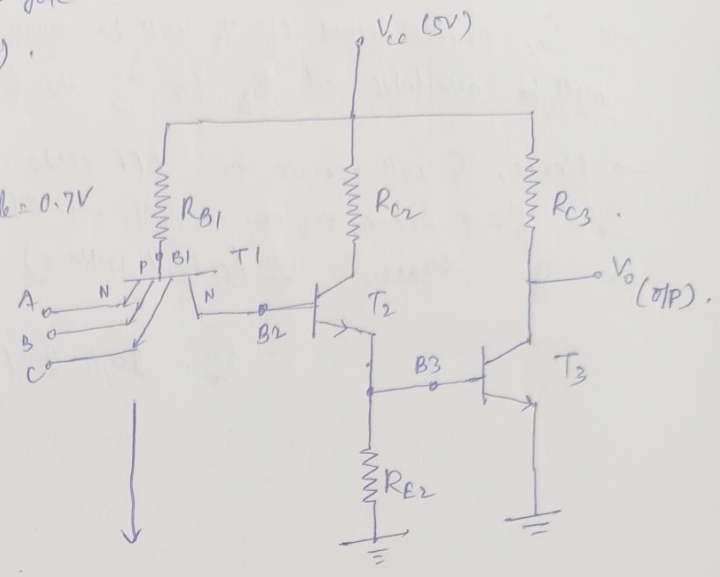
Diode { Voltage across a conducting diode = 0.7V
Cut-in voltage, = 0.6V

Transistor,

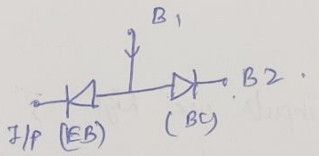
Cut-in voltage = 0.5V

$V_{BE,sat.}$ = 0.8V

$V_{CE,sat.}$ = 0.2V



T_1

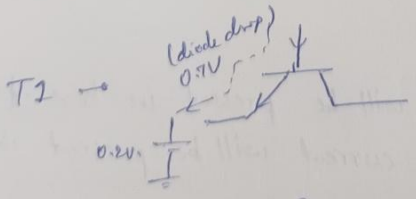


Case-I. → logic 0 is applied [Low i/p).

→ i/p = 0.2V. (logic 0), diode . EB is F.B & C.B j^n. is RB.

→ Transistor will work in active region,

→



at B_1.

→ (0.2+0.7)V = 0.9V ~~drop~~ is from Emitter to base junction.

→ CB j^n. of T_1 is R.B, so sufficient voltage will not be available at B_2 for T_2 ~~be~~ to be in ON state.

→ Transistor T_2 will be in OFF-state.

→ So, emitter current of T_2 will be zero. Hence no sufficient voltage will be available at B_3 for T_3 to be in ON state.

→ Hence, T_3 will remain in OFF state.

→ T_1 → Active region, T_2 & T_3 → OFF state.

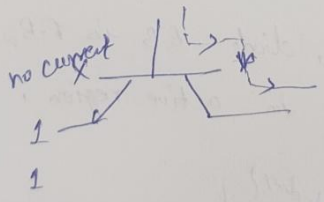
→ Hence, V_0 (output voltage) = V_{CC} (High).

V_0 = Logic 1 (5V).

Case-II: All inputs are high, A, B, C = logic 1.

→ T_1 → EB jn is in Reverse biased. & BC jn is F.B.

→ Current will flow in Base collector jn.



→ Sufficient ~~current~~ voltage will be present in base terminal so that T_2, Emitter current will be present in T_2.

→ So, sufficient voltage will be present at B_3 for T_3 to be in ON state.

→ Hence, T_3 will be short ckt.

→ V_0 (output voltage) = Logic 0.

Assignment-I (CO1)

1. Convert the following-
   a) $(101101.10101)_2$ to ( )$_{10}$
   b) $(195.25)_{10}$ to ( )$_2$
   c) $(2325)_8$ to ( )$_2$
   d) $(105)_{16}$ to ( )$_8$
   e) $(1228)_{10}$ to ( )$_{16}$
   f) $(600)_{10}$ to ( )$_{16}$
   g) $(A3BH)_{16}$ to ( )$_{10}$
   h) $(11011.011)_2$ to ( )$_{16}$
   i) $(A6BF5)_{16}$ to ( )$_2$
   j) $(7864)_{10}$ to ( )$_{16}$
   k) $(10111101)_{Gray}$ to ( )$_{Binary}$
   l) $(1110011010)_{Binary}$ to ( )$_{Gray}$
2. Subtract $(1010)_2$ from $(1000)_2$ using 1's compliment method.
3. Subtract $(1010)_2$ from $(1000)_2$ using 2's compliment method.
4. Subtract $(1010)_2$ from $(1111)_2$ using 2's compliment method.
5. What are the characteristics of digital IC? Describe each one of them in detail.
6. Simplify the following Boolean expressions-
   a) $(A + \overline{B} + \overline{C})(A + \overline{B} + C)(A + B + \overline{C})$
   b) AB + A(B + C) + B(B + C)
   c) $\overline{\overline{A + B\overline{C}} + D(\overline{E + F})}$
   d) $(A+B)\cdot(A+\overline{A}\,\overline{B})\cdot C + \overline{\overline{A}\cdot(B+\overline{C})} + \overline{A}\cdot B + A\cdot B\cdot C$
   e) $(A+A\cdot\overline{B})\cdot(A\cdot C + A\cdot\overline{C}\cdot(\overline{A}+B))\cdot(B+C)$
7. Describe the working of TTL circuit with the help of a neat diagram.
8. Write short notes on-
   a) Schottky TTL
   b) CMOS logic

Assignment-II (CO2)

1. Convert the following Boolean expression into standard SOP form:

$$A\overline{B}C + \overline{A}\overline{B} + AB\overline{C}D$$

2. Convert the following Boolean expression into standard POS form:

$$(A + \overline{B} + C)(\overline{B} + C + \overline{D})(A + \overline{B} + \overline{C} + D)$$

Moderation Form

पूर्णियाँ अभियंत्रण महाविद्यालय
पूर्णियाँ - ८५४३०३

PURNEA COLLEGE OF ENGINEERINGPURNEA-854303

MODERATION FORM
MID-SEMESTER QUESTION PAPER QUALITY ANALYSIS

Faculty Name:	Tabish Shanu	Sem:	4th.
Subject Name:	Digital Electronics	Max. Marks:	20
Subject Code:	100403	Duration:	2hrs.
DEPARTMENT:	Electrical Engineering		

S.No.	Assessment Parameters	Remarks		
1	Are the Course Outcomes defined for course, met in the questions asked	✓ Yes / No		
2	Are the CO in-line with Blooms Taxonomy level and specified in the Question Paper	✓ Yes / No		
3	Is the weightage of questions set for COs specified in the QP appropriate	Yes / No		remarks
			CO 1	YES
			CO 2	YES.
			CO 3	
			CO 4	
			CO 5	
4	Rate the strength of questions set	STRENGTH		remarks
		Easy		30%.
		Medium		50%.
		Tough		20%.
5	Time specified is sufficient for the students to attempt them comfortably	Yes / No		YES
6	Does the QP includes mandatory question	Yes / No		YES
7	Does the QP includes innovative question	Yes / No		YES
8	Does the QP is in line with University QP format	Yes / No		YES.
Any Other Remarks		—		

16/11/2024 Tabish Shanu. Name & Signature of QP setting Faculty	16/11/2024 Name & Signature of Moderating Faculty	16/11/24 Name & Signature of Departmental Academic Co-ordinator

Electrical Engineering Department
Mid-Semester Examination- November 2024

Duration: 2 Hrs | Semester: 4th (EE) | Full Marks: 20 | Subject: DE
Session-2024-25 | Batch- 2022-26 | Date: 21/11/2024

CO1	To understand digital logic principles, IC gates, and interfacing in practical circuits.
CO2	To apply logic representation, simplification, and digital circuit components for problem-solving.
CO3	To understand flip-flops, counters, and memory elements for digital circuit design.
CO4	To analyse digital-to-analog and analog-to-digital converters in signal processing systems.
CO5	To understand memory organization, types, and programmable devices in digital systems.

(*Answer any four question. Each question carries five marks.*)

1. Convert the following- (CO1)
   a) $(101101.10101)_2$ to $(\ )_{10}$
   b) $(195.25)_{10}$ to $(\ )_2$
   c) $(2325)_8$ to $(\ )_2$
   d) $(A3B)_{16}$ to $(\ )_{10}$
   e) $(11011.011)_2$ to $(\ )_{16}$
2. What are the characteristics of digital IC? Describe each one of them in detail. (CO1)
3. Simplify the following Boolean expressions- (CO1)
   a) AB + A(B + C) + B(B + C)
   b) $\overline{\overline{A + B\overline{C}} + D(\overline{E + \overline{F}})}$
4. Write short notes on- (CO1)
   a) Working of TTL circuit
   b) CMOS logic
5. a) Convert the following Boolean expression into standard SOP form: (CO2)

   $A\overline{B}C + \overline{A}\overline{B} + AB\overline{C}D$

   b) Convert the following Boolean expression into standard POS form:

Previous Year Question Paper (2022)

Code : 100403

B.Tech 4th Semester Exam., 2022

(New Course)

DIGITAL ELECTRONICS

Time : 3 hours *Full Marks* : 70

Instructions :

(i) The marks are indicated in the right-hand margin.

*(ii) There are **NINE** questions in this paper.*

*(iii) Attempt **FIVE** questions in all.*

(iv) Question No. 1 is compulsory.

1. Answer any *seven* of the following : 2×7=14

(a) What is the next number in the following octal counting sequence?

724, 725, 726, 727, ____

(b) What do you mean by a positive logic system and a negative logic system?

(c) Subtract using 9's complement :

745.81 – 436.62

(d) The following operation is correct for at least one number system. Find the correct number system :

1234 + 5432 = 6666

(e) What is a tri-state logic?

(f) Which are the fastest logic family and the slowest logic family?

(g) Which memory technology needs the least power?

(h) What is a register? What is a shift register?

(i) What is a master-slave flip-flop?

(j) Fill in the blank :

$(100101000111)_{(BCD)} = (\_\_\_\_)_{10}$

2. *(a)* Which of the following are analog quantities and which are digital?

Number of atoms in a sample of material, Altitude of an aircraft, Pressure in a bicycle tire, Current through a speaker, and Timer setting on a microwave oven.

(b) What do you mean by self-complementing code? Write two self-complementing codes.

(c) If the waveforms *A* and *B* shown in Fig. 1 are applied to a two-input XOR gate, determine the output waveform :

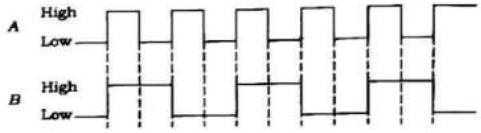


Fig. 1 4+4+6

3. *(a)* Perform the following in excess-3 code using the 10's complement method :

239 – 597

(b) Design and implement a 4-bit binary to Gray converter.

(c) Reduce the following expression using K-map and implement it in AOI logic as well as in NOR logic :

$F = \Pi M(0, 1, 2, 3, 4, 7)$ 5+4+5

4. *(a)* Reduce the following expression and implement it using universal logic gate :

$\Sigma m(1, 5, 6, 12, 13, 14) + d(2, 4)$

(b) Use a multiplexer to implement the logic function $F = A \oplus B \oplus C$. 7+7

5. *(a)* Determine the *Q*-output waveform if the inputs shown in Fig. 2 are applied to the gated *D*-latch which is initially RESET :

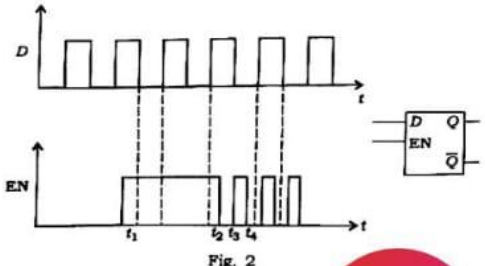


Fig. 2

(b) Design the conversion cir flip-flop to *J-K* flip-flop.

6. (a) What is basic difference between a counter and a shift register?

(b) With neat diagrams, explain the working of the following types of shift registers :

(i) Serial-in, serial-out

(ii) Serial-in, parallel-out

(c) Design and implement a mod-10 asynchronous counter using T flip-flops. 3+6+5

7. (a) Design and implement a synchronous 3-bit up/down counter using J-K flip-flops.

(b) Determine the resolution of—

(i) 6-bit DAC;

(ii) 12-bit DAC

in terms of percentage.

(c) What is the resolution of a 9-bit DAC which uses a ladder network? What is this resolution expressed as a percentage? If the full-scale output voltage of this converter is +5 V, what is resolution in volts? 5+4+5

8. (a) For the 4-bit weighted resistor DAC shown in Fig. 3, determine the—

(i) weight of each input bit if the inputs are 0 V and 5 V;

(ii) full-scale output if $R_f = R = 1\,k\Omega$.

Also, find the full-scale output if R_f is changed to $500\,\Omega$:

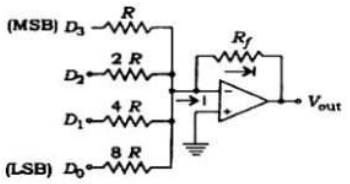


Fig. 3

(b) What is a PLD? What do '×' and 'dot' represent on a PLD diagram? 9+5

9. (a) What are the different technologies used for the fabrication of ROM memories? Determine how many 16K × 4 memory circuits would be required to construct each of the following memories :

(i) 256K × 8

(ii) 128K × 16

(b) Define Memory cell, Address and Byte.

(c) Using the simplified connection format of a PLA, show how an 8 × 1 PROM should be programmed to implement the logic function

$F = \Sigma m(1, 4, 5, 7)$ 4½+4½+5

★ ★ ★

Previous Year Question Paper (2023)

Bihar Engineering University, Patna
End Semester Examination -2023

Course: B.Tech | *Semester: IV* | *Time: 03 Hours*
Code: 100403 | *Subject: Digital Electronics* | *Full Marks: 70*

Instructions:-

(i) The marks are indicated in the right-hand margin.
*(ii) There are **NINE** questions in this paper.*
*(iii) Attempt **FIVE** questions in all.*
*(iv) Question No. **1** is compulsory.*

Q.1 ***Answer any seven Question only:*** **[2 x 7 = 14]**

(a) Convert the Decimal number (108.025) to their binary equivalent.
(b) Draw Truth table of JK flip flop.
(c) Draw the truth table and logic circuit of Half-adder.
(d) Write the difference between combinational & Sequential circuit.
(e) Draw timing diagram of SR flip-flop.
(f) Find 2's complement of 1011011.
(g) Number of 2:1 mux requires designing 256:1 mux is .....
(h) Add hexadecimal number 2ABC & 98F2.
(i) Discuss Universal gates.
(j) What is the use of K-map?

Q.2 Implement the following function using only NAND gate **[14]**
$F(A,B,C)=\sum m(0,1,2,3,7)$.

Q.3 (a) Realize XNOR logic function using NAND gate only. **[7]**
(b) Simplify $Y= ABC + AB\overline{C} + A\overline{B}C$ **[7]**

Q.4 A logic circuit has four inputs A,B,C,D and output Y. Y=1 when A & B are both 1,subjected to the condition that C and D are both low or both high. Design the logic circuit. **[14]**

Q.5 Explain Master-slave flip flop. What are race around condition?. How it can be circumvented with the help of Master-slave flip flop. **[14]**

Q.6 (a) Design 8 to 3 line Encoder circuit. **[7]**
(b) Implement NAND gate using TTL logic family. **[7]**

Q.7 Summarize the design procedure for a synchronous sequential circuit. **[14]**

Q.8 (a) Explain the working of R-2R Ladder DAC. **[7]**
(b) Design 3-bit binary counter using T flip-flop. **[7]**

Q.9 Write short notes on the following: **[7*2=14]**
(a) Binary Parallel Adder
(b) Digital IC logic families

List of Weak Students

LIST OF WEEK STUDENTS			
Sl No	**Registration No**	**Name**	**Mid Term Marks (20)**
1	21103131033	VIVEK KUMAR	5
2	22103131001	ROHIT RAJ	4
3	22103131042	PINTU KUMAR YADAV	5
4	23103131903	SATIMALA KUMARI	4

COURSE END SURVEY

Digital Electronics (2022-26 batch)

COURSE END SURVEY DIGITAL ELECTRONICS (2022-26 Batch)								
Sl. No	Registration No.	Name	CO1	CO2	CO3	CO4	CO5	Signature
1	21103131001	SAHIL KUMAR	5	4	5	5	5	Sahil Kumar
2	21103131002	NITISH KUMAR	4	4	4	5	5	AB
3	21103131004	RAJ KUMAR	5	5	5	5	5	Raj Kumar.
4	21103131012	NEHA KUMARI	4	4	4	4	4	Neha Kumari
5	21103131017	HARIOM KUMAR	4	5	5	5	5	AB
6	21103131024	SUPRIYA KUMARI	4	4	4	5	5	Supriya Kumari
7	21103131026	PRATIK KUMAR	5	5	5	4	4	AB
8	21103131030	PANKAJ KUAMR	4	4	4	4	4	Pankaj
9	21103131033	VIVEK KUMAR	5	5	5	5	5	Vivek Kumar
10	21103131047	HARSHIT KUMAR	4	5	4	4	4	Harshit Kumar
11	21103131053	ANJALI PRIYA	5	4	5	5	5	Anjali Priya
12	22103131001	ROHIT RAJ	4	5	4	5	5	Rohit Raj
13	22103131002	SAMEER	5	5	3	5	4	Sameer
14	22103131003	ASRAR AHMAD	4	4	4	5	5	Asrar Ahmad.
15	22103131004	ANUBHAV KUMAR	5	4	5	5	5	AB
16	22103131006	VIKASH KUMAR	5	5	4	4	4	Vikash Kumar
17	22103131007	PRABHAT KUMAR	5	5	5	5	5	AB
18	22103131008	ASHISH AMAN	4	4	4	4	4	AB
19	22103131009	ANUKRITI	5	5	4	4	4	AB
20	22103131010	SADAN KUMAR	4	4	5	5	5	Sadan Kumar
21	22103131011	MANNU KUMAR	4	5	4	5	5	Mannu Shaly
22	22103131012	ANSHU PRIYA	5	5	5	5	5	Anshu Priya
23	22103131013	RAVISHANKAR KUMAR	5	5	4	4	4	Ravishankar kumar
24	22103131014	MANISH KUMAR	4	4	5	5	5	Manish Kumar
25	22103131015	MONU KUMAR	5	4	5	5	5	Monu Kumar
26	22103131017	AMAN KUMAR	4	5	4	4	4	Aman kumar
27	22103131018	SHIVANI KUMARI	5	4	5	5	5	Shivani Kumari
28	22103131019	BADAL KUMAR	5	5	4	5	4	Badal kumar
29	22103131020	ABHINAY KUMAR	5	4	4	4	4	Abhinay Kumar
30	22103131023	ANUSHKA SINGH	5	5	5	5	5	Anushka Singh
31	22103131025	UTKARSH JHA	4	4	4	5	5	Utkarsh Jha
32	22103131027	KOMAL KUMAR	5	5	5	5	5	AB

33	22103131029	SONI PRIYA	4	5	4	4	4	Soni Priya
34	22103131030	GHANSHYAM KUMAR	5	4	5	5	5	Ghanshyam kumar
35	22103131032	SUMAN KUMAR	4	5	4	4	4	Suman Kumar
36	22103131033	SHIVAM KUMAR	5	5	4	4	4	Shivam Kumar
37	22103131034	VIJAY KUMAR	5	4	5	5	5	Vijay Kumar
38	22103131035	ASHISH KUMAR	4	4	4	5	5	Ashish Kumar
39	22103131036	ANKIT RAJ PRINCE	5	5	5	5	3	Ankit Raj
40	22103131037	NISHA KUMARI	4	5	5	4	4	Nisha Kumari
41	22103131038	ROHIT KUMAR	5	4	4	4	4	Rohit Kr.
42	22103131039	SAKSHI SUMAN	4	5	5	5	5	Sakshi Suman
43	22103131040	ARYAN KUMAR	5	4	4	5	5	Aryan Kr.
44	22103131042	PINTU KUMAR YADAV	4	5	5	5	5	Pintu Yadav
45	22103131043	PARMESHWARI BHARTI	5	5	4	4	4	Parmeshwari Bharti
46	22103131044	ABHAY KUMAR	5	4	5	5	5	Abhay Kumar
47	22103131911	SILKI KUMARI	5	4	4	4	4	Silki Kumari
48	23103131901	NEHA KUMARI	4	4	5	5	5	Neha Kumari
49	23103131902	YASH RAJ	5	5	4	4	4	Yash Raj
50	23103131903	SATIMALA KUMARI	5	4	5	5	5	Satimala Kumari
51	23103131904	AVINASH KUMAR	5	5	5	5	5	Avinash Kumar
52	23103131905	PRIYANSHU BHARTI	4	5	4	4	4	AB
53	23103131906	SHIVANI KUMARI	5	4	5	5	5	AB
54	23103131907	VIJAY KUMAR	5	4	4	4	4	AB
55	23103131908	KHUSHI ANAND	4	5	4	4	4	Khushi Anand
56	23103131909	ANUPRIYA KUMARI	5	4	5	5	5	AB
57	23103131910	MUSKAN KUMARI	4	5	4	5	5	Muskan Kumari
58	23103131911	RAJLAKSHMI	5	5	5	5	5	Rajlakshmi
59	23103131912	SHWETA KUMARI	4	5	4	4	4	Shweta Kumari
60	23103131913	YAMIKA BHARTI	5	5	5	5	5	Yamika Bharti
61	23103131914	RITESH KUMAR	5	5	4	4	4	Ritesh Kumar
62	23103131915	RAMESH KUMAR SAH	4	4	5	5	5	Ramesh Kumar Sah
63	23103131916	KRISHAN KUMAR	5	4	5	4	4	Krishan Kumar
64	23103131917	KUNDAN KUMAR YADAV	5	5	4	4	4	Kundan Kr. Yadav
65	23103131918	KANHAIYA KUMAR	4	4	5	5	5	AB
66	23103131919	VIKAS KUMAR RAM	5	5	5	5	5	Vikas Kumar

Mid-Semester Marks-

S.N	Registration No.	Student Name	Attendance (5)	Class Test (5)	Mid Sem(20)	Out of Mark 30
1	21103131001	SAHIL KUMAR	5	5	13	23
2	21103131002	NITISH KUMAR	5	5	11	21
3	21103131004	RAJ KUMAR	4	5	10	19
4	21103131012	NEHA KUMARI	5	5	15	25
5	21103131017	HARIOM KUMAR	5	5	8	18
6	21103131024	SUPRIYA KUMARI	5	5	8	18
7	21103131026	PRATIK KUMAR	4	5	10	19
8	21103131030	PANKAJ KUAMR	4	5	15	24
9	21103131033	VIVEK KUMAR	5	5	5	15
10	21103131047	HARSHIT KUMAR	4	5	10	19
11	21103131053	ANJALI PRIYA	5	5	17	27
12	22103131001	ROHIT RAJ	5	5	4	14
13	22103131002	SAMEER	4	5	13	22
14	22103131003	ASRAR AHMAD	5	5	6	16
15	22103131004	ANUBHAV KUMAR	4	4	19	27
16	22103131006	VIKASH KUMAR	4	5	17	26
17	22103131007	PRABHAT KUMAR	5	5	15	25
18	22103131008	ASHISH AMAN	4	4	19	27
19	22103131009	ANUKRITI	5	5	10	20
20	22103131010	SADAN KUMAR	5	5	16	26
21	22103131011	MANNU KUMAR	5	5	16	26
22	22103131012	ANSHU PRIYA	4	4	20	28
23	22103131013	RAVISHANKAR KUMAR	4	5	10	19
24	22103131014	MANISH KUMAR	5	5	9	19
25	22103131015	MONU KUMAR	5	5	10	20
26	22103131017	AMAN KUMAR	5	5	15	25
27	22103131018	SHIVANI KUMARI	5	5	13	23
28	22103131019	BADAL KUMAR	5	5	16	26
29	22103131020	ABHINAY KUMAR	4	5	18	27
30	22103131023	ANUSHKA SINGH	4	5	18	27
31	22103131025	UTKARSH JHA	5	5	7	17

32	22103131027	KOMAL KUMAR	5	5	9	19
33	22103131029	SONI PRIYA	4	4	20	28
34	22103131030	GHANSHYAM KUMAR	5	5	15	25
35	22103131032	SUMAN KUMAR	4	5	17	26
36	22103131033	SHIVAM KUMAR	5	5	11	21
37	22103131034	VIJAY KUMAR	5	4	16	25
38	22103131035	ASHISH KUMAR	4	5	17	26
39	22103131036	ANKIT RAJ PRINCE	5	5	15	25
40	22103131037	NISHA KUMARI	4	4	19	27
41	22103131038	ROHIT KUMAR	4	4	19	27
42	22103131039	SAKSHI SUMAN	4	5	18	27
43	22103131040	ARYAN KUMAR	5	5	13	23
44	22103131042	PINTU KUMAR YADAV	5	5	5	15
45	22103131043	PARMESHWARI BHARTI	4	4	19	27
46	22103131044	ABHAY KUMAR	5	5	15	25
47	22103131911	SILKI KUMARI	4	5	18	27
48	23103131901	NEHA KUMARI	4	4	19	27
49	23103131902	YASH RAJ	4	5	16	25
50	23103131903	SATIMALA KUMARI	5	5	4	14
51	23103131904	AVINASH KUMAR	4	5	18	27
52	23103131905	PRIYANSHU BHARTI	5	5	11	21
53	23103131906	SHIVANI KUMARI	4	4	19	27
54	23103131907	VIJAY KUMAR	5	5	13	23
55	23103131908	KHUSHI ANAND	4	4	19	27
56	23103131909	ANUPRIYA KUMARI	5	5	8	18
57	23103131910	MUSKAN KUMARI	4	4	20	28
58	23103131911	RAJLAKSHMI	4	4	20	28
59	23103131912	SHWETA KUMARI	4	4	20	28
60	23103131913	YAMIKA BHARTI	5	5	14	24
61	23103131914	RITESH KUMAR	5	5	14	24
62	23103131915	RAMESH KUMAR SAH	5	5	12	22
63	23103131916	KRISHAN KUMAR	4	5	17	26
64	23103131917	KUNDAN KUMAR YADAV	4	4	19	27
65	23103131918	KANHAIYA KUMAR	5	5	13	23
66	23103131919	VIKAS KUMAR RAM	5	5	14	24

CO ATTAINMENT ANALYSIS AND PO/PSO ATTAINMENT

CO Attainment Through Mid Semester Exam

CO		CO1	CO1	CO1	CO1	CO2	Total Marks
QUES		1	2	3	4	5	
Max mark	Reg. No.	5	5	5	5	5	20
21103131001	SAHIL KUMAR		4	3	3	3	13
21103131002	NITISH KUMAR	4	2	3	2		11
21103131004	RAJ KUMAR	3	2		3	2	10
21103131012	NEHA KUMARI	4		2	4	5	15
21103131017	HARIOM KUMAR		3	3	2		8
21103131024	SUPRIYA KUMARI		2	3		3	8
21103131026	PRATIK KUMAR	1	2		3	4	10
21103131030	PANKAJ KUAMR	4	3		3	5	15
21103131033	VIVEK KUMAR			3	2		5
21103131047	HARSHIT KUMAR		2		3	5	10
21103131053	ANJALI PRIYA	4	4		4	5	17
22103131001	ROHIT RAJ	2			2		4
22103131002	SAMEER	1	4		3	5	13
22103131003	ASRAR AHMAD		3		1	2	6
22103131004	ANUBHAV KUMAR	5	5		4	5	19
22103131006	VIKASH KUMAR	5	4	4	4		17
22103131007	PRABHAT KUMAR	3	4	5	3		15
22103131008	ASHISH AMAN	5	5	4		5	19
22103131009	ANUKRITI	3		5		2	10
22103131010	SADAN KUMAR	5		4	2	5	16
22103131011	MANNU KUMAR	5	4	4		3	16
22103131012	ANSHU PRIYA	5	5	5		5	20
22103131013	RAVISHANKAR KUMAR	4	5			1	10
22103131014	MANISH KUMAR	2	1		3	3	9

22103131015	MONU KUMAR	**2**	**3**		**3**	**2**	**10**
22103131017	AMAN KUMAR	**3**	**4**	**5**	**3**		**15**
22103131018	SHIVANI KUMARI		**3**	**5**		**5**	**13**
22103131019	BADAL KUMAR	**4**	**4**		**4**	**4**	**16**
22103131020	ABHINAY KUMAR	**4**		**5**	**4**	**5**	**18**
22103131023	ANUSHKA SINGH	**4**	**4**	**5**		**5**	**18**
22103131025	UTKARSH JHA		**3**	**2**		**2**	**7**
22103131027	KOMAL KUMAR	**3**	**2**	**3**		**2**	**9**
22103131029	SONI PRIYA	**5**	**5**	**5**	**5**		**20**
22103131030	GHANSHYAM KUMAR		**4**	**5**	**4**	**2**	**15**
22103131032	SUMAN KUMAR	**4**		**5**	**3**	**5**	**17**
22103131033	SHIVAM KUMAR	**4**		**3**	**4**		**11**
22103131034	VIJAY KUMAR	**4**	**4**	**5**		**3**	**16**
22103131035	ASHISH KUMAR	**4**	**4**	**5**	**4**		**17**
22103131036	ANKIT RAJ PRINCE	**4**	**3**	**4**		**4**	**15**
22103131037	NISHA KUMARI	**5**	**4**	**5**		**5**	**19**
22103131038	ROHIT KUMAR	**5**		**5**	**4**	**5**	**19**
22103131039	SAKSHI SUMAN	**5**		**5**	**3**	**5**	**18**
22103131040	ARYAN KUMAR			**5**	**3**	**5**	**13**
22103131042	PINTU KUMAR YADAV		**2**		**3**		**5**
22103131043	PARMESHWARI BHARTI	**4**	**5**	**5**	**5**		**19**
22103131044	ABHAY KUMAR	**4**		**3**	**3**	**5**	**15**
22103131911	SILKI KUMARI	**4**	**4**		**5**	**5**	**18**
23103131901	NEHA KUMARI	**5**	**4**	**5**		**5**	**19**
23103131902	YASH RAJ	**5**	**4**		**4**	**3**	**16**
23103131903	SATIMALA KUMARI	**1**		**1**		**2**	**4**
23103131904	AVINASH KUMAR	**5**	**4**		**4**	**5**	**18**
23103131905	PRIYANSHU BHARTI	**3**	**4**		**4**		**11**
23103131906	SHIVANI KUMARI	**5**	**4**	**5**		**5**	**19**
23103131907	VIJAY KUMAR		**3**	**2**	**3**	**5**	**13**

23103131908	KHUSHI ANAND	**5**	**5**		**5**	**4**	**19**
23103131909	ANUPRIYA KUMARI	**2**	**2**		**2**	**2**	**8**
23103131910	MUSKAN KUMARI	**5**	**5**	**5**		**5**	**20**
23103131911	RAJLAKSHMI	**5**	**5**		**5**	**5**	**20**
23103131912	SHWETA KUMARI	**5**	**5**	**5**		**5**	**20**
23103131913	YAMIKA BHARTI	**3**	**3**		**3**	**5**	**14**
23103131914	RITESH KUMAR	**2**	**4**		**3**	**5**	**14**
23103131915	RAMESH KUMAR SAH	**2**	**2**		**5**	**3**	**12**
23103131916	KRISHAN KUMAR	**4**	**3**		**5**	**5**	**17**
23103131917	KUNDAN KUMAR YADAV	**5**	**5**		**5**	**4**	**19**
23103131918	KANHAIYA KUMAR	**5**		**4**	**3**	**1**	**13**
23103131919	VIKAS KUMAR RAM	**3**	**3**	**4**		**4**	**14**
	Average Marks						

CO ATTAINMENT THROUGH ASSIGNMENT

Max mark	Reg. No.	Assignment marks (5)
21103131001	SAHIL KUMAR	5
21103131002	NITISH KUMAR	5
21103131004	RAJ KUMAR	5
21103131012	NEHA KUMARI	5
21103131017	HARIOM KUMAR	5
21103131024	SUPRIYA KUMARI	5
21103131026	PRATIK KUMAR	5
21103131030	PANKAJ KUAMR	5
21103131033	VIVEK KUMAR	5
21103131047	HARSHIT KUMAR	5
21103131053	ANJALI PRIYA	5
22103131001	ROHIT RAJ	5
22103131002	SAMEER	5
22103131003	ASRAR AHMAD	5

22103131004	ANUBHAV KUMAR	4
22103131006	VIKASH KUMAR	5
22103131007	PRABHAT KUMAR	5
22103131008	ASHISH AMAN	4
22103131009	ANUKRITI	5
22103131010	SADAN KUMAR	5
22103131011	MANNU KUMAR	5
22103131012	ANSHU PRIYA	4
22103131013	RAVISHANKAR KUMAR	5
22103131014	MANISH KUMAR	5
22103131015	MONU KUMAR	5
22103131017	AMAN KUMAR	5
22103131018	SHIVANI KUMARI	5
22103131019	BADAL KUMAR	5
22103131020	ABHINAY KUMAR	5
22103131023	ANUSHKA SINGH	5
22103131025	UTKARSH JHA	5
22103131027	KOMAL KUMAR	5
22103131029	SONI PRIYA	4
22103131030	GHANSHYAM KUMAR	5
22103131032	SUMAN KUMAR	5
22103131033	SHIVAM KUMAR	5
22103131034	VIJAY KUMAR	4
22103131035	ASHISH KUMAR	5
22103131036	ANKIT RAJ PRINCE	5
22103131037	NISHA KUMARI	4
22103131038	ROHIT KUMAR	4
22103131039	SAKSHI SUMAN	5
22103131040	ARYAN KUMAR	5
22103131042	PINTU KUMAR YADAV	5
22103131043	PARMESHWARI	4

	BHARTI	
22103131044	ABHAY KUMAR	5
22103131911	SILKI KUMARI	5
23103131901	NEHA KUMARI	4
23103131902	YASH RAJ	5
23103131903	SATIMALA KUMARI	5
23103131904	AVINASH KUMAR	5
23103131905	PRIYANSHU BHARTI	5
23103131906	SHIVANI KUMARI	4
23103131907	VIJAY KUMAR	5
23103131908	KHUSHI ANAND	4
23103131909	ANUPRIYA KUMARI	5
23103131910	MUSKAN KUMARI	4
23103131911	RAJLAKSHMI	4
23103131912	SHWETA KUMARI	4
23103131913	YAMIKA BHARTI	5
23103131914	RITESH KUMAR	5
23103131915	RAMESH KUMAR SAH	5
23103131916	KRISHAN KUMAR	5
23103131917	KUNDAN KUMAR YADAV	4
23103131918	KANHAIYA KUMAR	5
23103131919	VIKAS KUMAR RAM	5

CO ATTAINMENT THROUGH ATTENDANCE

Name	Reg. No.	Attendance Marks (5)
21103131001	SAHIL KUMAR	5
21103131002	NITISH KUMAR	5
21103131004	RAJ KUMAR	4
21103131012	NEHA KUMARI	5
21103131017	HARIOM KUMAR	5
21103131024	SUPRIYA KUMARI	5

21103131026	PRATIK KUMAR	4
21103131030	PANKAJ KUAMR	4
21103131033	VIVEK KUMAR	5
21103131047	HARSHIT KUMAR	4
21103131053	ANJALI PRIYA	5
22103131001	ROHIT RAJ	5
22103131002	SAMEER	4
22103131003	ASRAR AHMAD	5
22103131004	ANUBHAV KUMAR	4
22103131006	VIKASH KUMAR	4
22103131007	PRABHAT KUMAR	5
22103131008	ASHISH AMAN	4
22103131009	ANUKRITI	5
22103131010	SADAN KUMAR	5
22103131011	MANNU KUMAR	5
22103131012	ANSHU PRIYA	4
22103131013	RAVISHANKAR KUMAR	4
22103131014	MANISH KUMAR	5
22103131015	MONU KUMAR	5
22103131017	AMAN KUMAR	5
22103131018	SHIVANI KUMARI	5
22103131019	BADAL KUMAR	5
22103131020	ABHINAY KUMAR	4
22103131023	ANUSHKA SINGH	4
22103131025	UTKARSH JHA	5
22103131027	KOMAL KUMAR	5
22103131029	SONI PRIYA	4
22103131030	GHANSHYAM KUMAR	5
22103131032	SUMAN KUMAR	4
22103131033	SHIVAM KUMAR	5
22103131034	VIJAY KUMAR	5

22103131035	ASHISH KUMAR	4
22103131036	ANKIT RAJ PRINCE	5
22103131037	NISHA KUMARI	4
22103131038	ROHIT KUMAR	4
22103131039	SAKSHI SUMAN	4
22103131040	ARYAN KUMAR	5
22103131042	PINTU KUMAR YADAV	5
22103131043	PARMESHWARI BHARTI	4
22103131044	ABHAY KUMAR	5
22103131911	SILKI KUMARI	4
23103131901	NEHA KUMARI	4
23103131902	YASH RAJ	4
23103131903	SATIMALA KUMARI	5
23103131904	AVINASH KUMAR	4
23103131905	PRIYANSHU BHARTI	5
23103131906	SHIVANI KUMARI	4
23103131907	VIJAY KUMAR	5
23103131908	KHUSHI ANAND	4
23103131909	ANUPRIYA KUMARI	5
23103131910	MUSKAN KUMARI	4
23103131911	RAJLAKSHMI	4
23103131912	SHWETA KUMARI	4
23103131913	YAMIKA BHARTI	5
23103131914	RITESH KUMAR	5
23103131915	RAMESH KUMAR SAH	5
23103131916	KRISHAN KUMAR	4
23103131917	KUNDAN KUMAR YADAV	4
23103131918	KANHAIYA KUMAR	5
23103131919	VIKAS KUMAR RAM	5

PO'S / PSO'S ADDRESSED BY COS & MAPPING STRENGTH WITH COURSE				
PO/PSO	**CO**	**No. of Sessions**	**% of session**	**Mapping Strength**
PO1	**CO1, CO2, CO3, CO4, CO5,**	**7+7+7+7+7**	**100**	**3**
PO2	**CO2, CO3, CO4, CO5,**	**7+7+7+7**	**80**	**3**
PO3	**CO1, CO2, CO3, CO4, CO5,**	**7+7+7+7+7**	**100**	**3**
PO4	**CO2, CO3, CO4, CO5,**	**7+7+7+7**	**80**	**3**
PO5	**CO1, CO2, CO3, CO4, CO5,**	**7+7+7+7+7**	**100**	**3**
PO6	**CO1, CO2, CO3, CO5,**	**7+7+7+7**	**80**	**3**
PO7	**CO2, CO4, CO5,**	**7+7+7**	**60**	**2**
PO8	**CO3, CO4,**	**7+7+**	**40**	**2**
PO9	**CO3, CO4, CO5,**	**7+7+7**	**60**	**2**
PO10	**CO2, CO4, CO5,**	**7+7+7**	**60**	**2**
PO11	**CO1, CO2, CO3, CO4, CO5,**	**7+7+7+7+7**	**100**	**3**
PO12	**CO1, CO2, CO3, CO4, CO5,**	**7+7+7+7+7**	**100**	**3**
PSO1	**CO1, CO2, CO3, CO5,**	**7+7+7+7**	**80**	**3**
PSO2	**CO2, CO3,**	**7+7+**	**40**	**2**
PSO3	**CO2, CO3, CO4, CO5,**	**7+7+7+7**	**80**	**3**

S. No.	Percentage of Session	Mapping Strength
1	**> 70**	**3**
2	**30 - 70**	**2**
3	**< 30**	**1**

CLASS AVERAGE IN CONTINUOUS INTERNAL EVALUATION				
CO	**Mid Term Exam (20)**	**Assignment (5)**	**Attendance (5)**	**Class Average(%)**
CO1	10.2	2.4	4.5	62.23%
CO2	3.2	2.4	4.6	81.39%
CO3	0.0	0.0	4.6	91.82%
CO4	0.0	0.0	4.6	91.82%
CO5	0.0	0.0	4.6	91.82%

Direct PO/PSO Attainment														
PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**
2.00	**2.00**	**2.00**	**2.00**	**2.00**	**2.00**	**2.00**	**2.00**	**2.00**	**2.00**	**2.00**	**2.00**	**2.00**	**2.00**	**2.00**

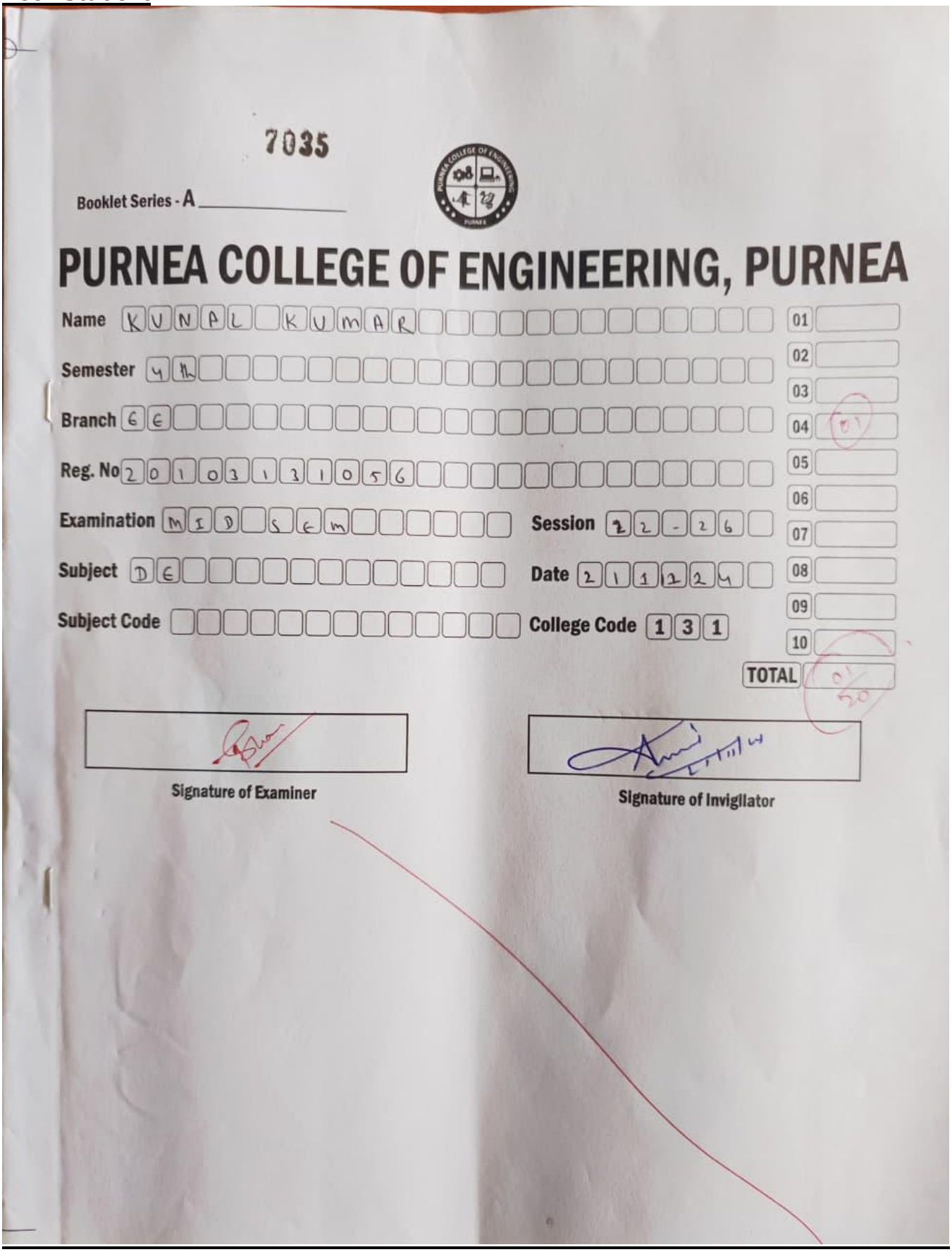
COURSE OUTCOME TARGET	
CO	**Target %**
CO1	**60%**
CO2	**65%**
CO3	**60%**
CO4	**70%**
CO5	**70%**

Direct CO Attainment			
(30% of Continuous internal evaluation + 70 % of end semester exam)			
CO	CIE (Class Avg. %)	ESE (Class Avg. %) (Same Value Assumed for all Cos)	Direct CO Attained (.30 OF CIE + .70 OF ESE)
CO1	62.23%	47.71%	**52.06%**
CO2	81.39%	47.71%	**57.81%**
CO3	91.82%	47.71%	**60.94%**
CO4	91.82%	47.71%	**60.94%**
CO5	91.82%	47.71%	**60.94%**

Total CO Attainment			
(90% of Direct CO Attainment + 10 % of Indirect CO Attainment)			
CO	Direct attained CO %	ndirectly Attained CO % (Course End Survey	Total CO Attained%
CO1	**52.06%**	71.82%	54.04%
CO2	**57.81%**	71.52%	59.18%
CO3	**60.94%**	81.82%	63.03%
CO4	**60.94%**	84.55%	63.30%
CO5	**60.94%**	84.55%	63.30%

CO Attainment Analysis					
CO	Target %	Attained %	Attainment gap (%)	Action Proposed to bridge the gap	Modification of target where achieved
CO1	**60.00%**	**54.04%**	**5.96%**	**Defined**	**60.00%**
CO2	**65%**	**59.18%**	**6%**	**Defined**	**65%**
CO3	**60%**	**63.03%**	**-3%**	**Attained**	**63.03%**
CO4	**70%**	**63.30%**	**7%**	**Defined**	**70%**
CO5	**70%**	**63.30%**	**7%**	**Defined**	**70%**

Poor Student



7035

Booklet Series - A

PURNEA COLLEGE OF ENGINEERING, PURNEA

Name KUNAL KUMAR

Semester 4TH

Branch EE

Reg. No 20103131056

Examination MIDSEM

Session 22-26

Subject DE

Date 21/12/24

Subject Code

College Code 131

01	
02	
03	
04	07
05	
06	
07	
08	
09	
10	
TOTAL	07/30

Signature of Examiner

Signature of Invigilator

(1)

(a) $(10110\,1.10102)_2$

$(110010.11)_{10}$ ✗

(b) $(195.25)_{10}$

$(176.08)_{10}$ ✗

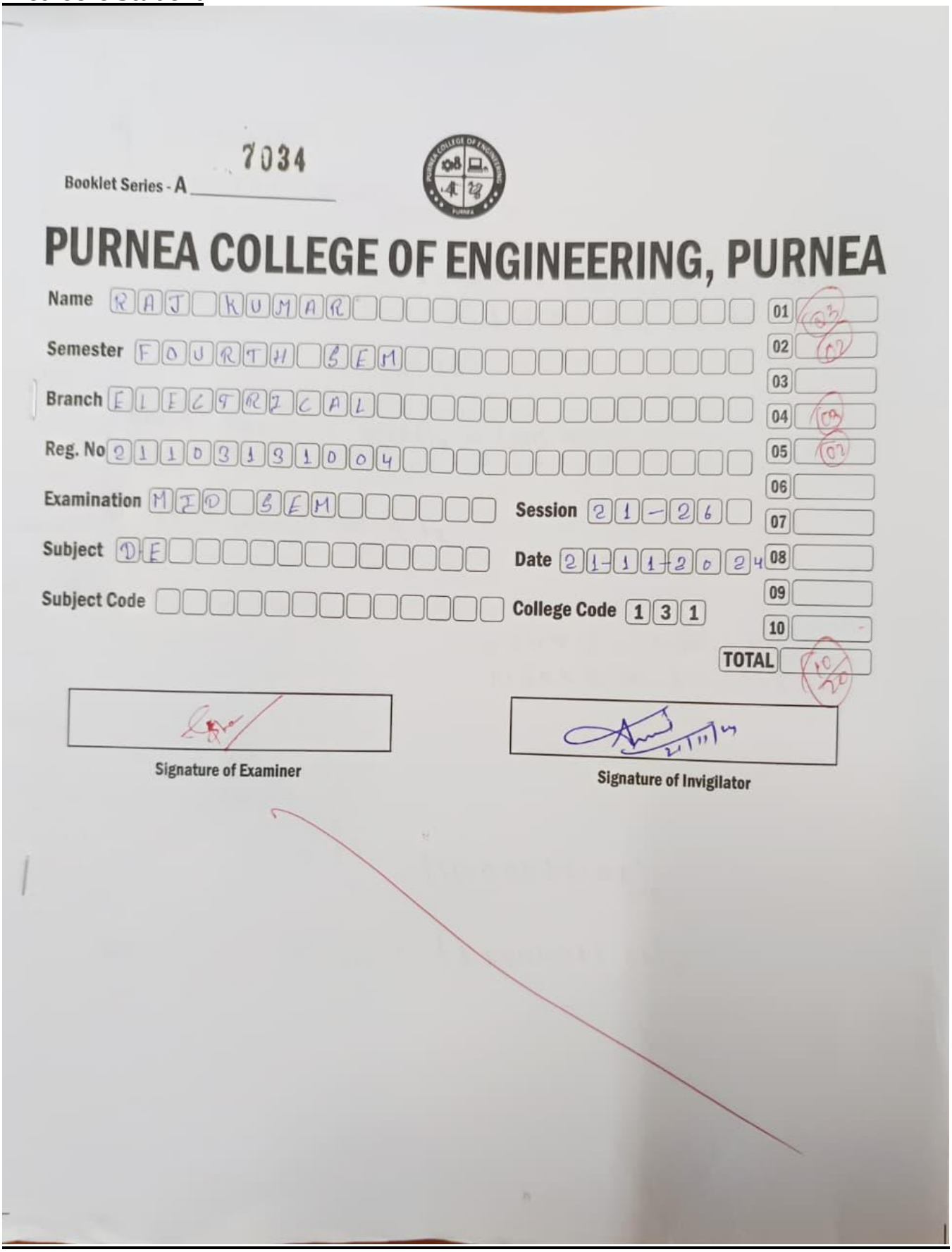
(c) $(2325)_8$

$(4714)_8$ ✓

(d) $(A_3B)_{16}$ ✓

(e) $(11011.011)_2$ ✓

Mediocre Student



Booklet Series - A 7034

PURNEA COLLEGE OF ENGINEERING, PURNEA

Name RAJ KUMAR

Semester FOURTH SEM

Branch ELECTRICAL

Reg. No 21103131004

Examination MID SEM

Session 21-26

Subject DE

Date 21-11-2024

Subject Code

College Code 131

01 02 03 04 05 06 07 08 09 10

TOTAL 10/20

Signature of Examiner

Signature of Invigilator

c) $(2325)_8$ to $(\ )_2$

8	2325	
8	290	5
8	36	2
	4	4

2	2325	
2	1162	1
2	581	0
2	290	1
2	145	0
2	72	1
2	36	0
2	18	0
2	9	0
2	4	1
2	2	0
	1	

~~$(100101)_2$~~

$(10100101011)_2$

c) $(11011.011)_2$ to $(\ )_{16}$

$0001\ 1011 . 0110)_2$

1 11 6

(B)

$(1B.6)_{16}$

d) $(AB8)_{16}$ to $(\ )_{10}$

1	10.311

(03)

4) CMOS logic

b) Complementary Metal oxid semiconductor logic is a circuit design that use complementary pair of P-channal and n-channal MOSFET to implement logic function.

Advantage

- extremely low Power asmption
- high speed
- high input
- high input impedance
- low output impedance

(01)

Disadvantage

- Higher complexity
- Reqwired dual Power supply
- Susceptible electrostatic disaster

1)

a) ~~(101101)~~

$(101101.10101)_2$ to $(\ )_{10}$

$1\times2^5+0\times2^4+1\times2^3+1\times2^2+0\times2^1+1\times2^0+1\times2^{-1}+0\times2^{-2}+1\times2^{-3}+0\times2^{-4}+1\times2^{-5}$

$32+0+8+4+0+1+0.5+0+0.125+0+0.3125$

45.9375

Hence $(101101.10101)_2 = (45.9375)_{10}$

b) $(195.25)_{10}$ to $(\ )_2$

2	195	
2	97	1
2	48	1
2	24	0
2	12	0
2	6	0
2	3	0
2	1	1

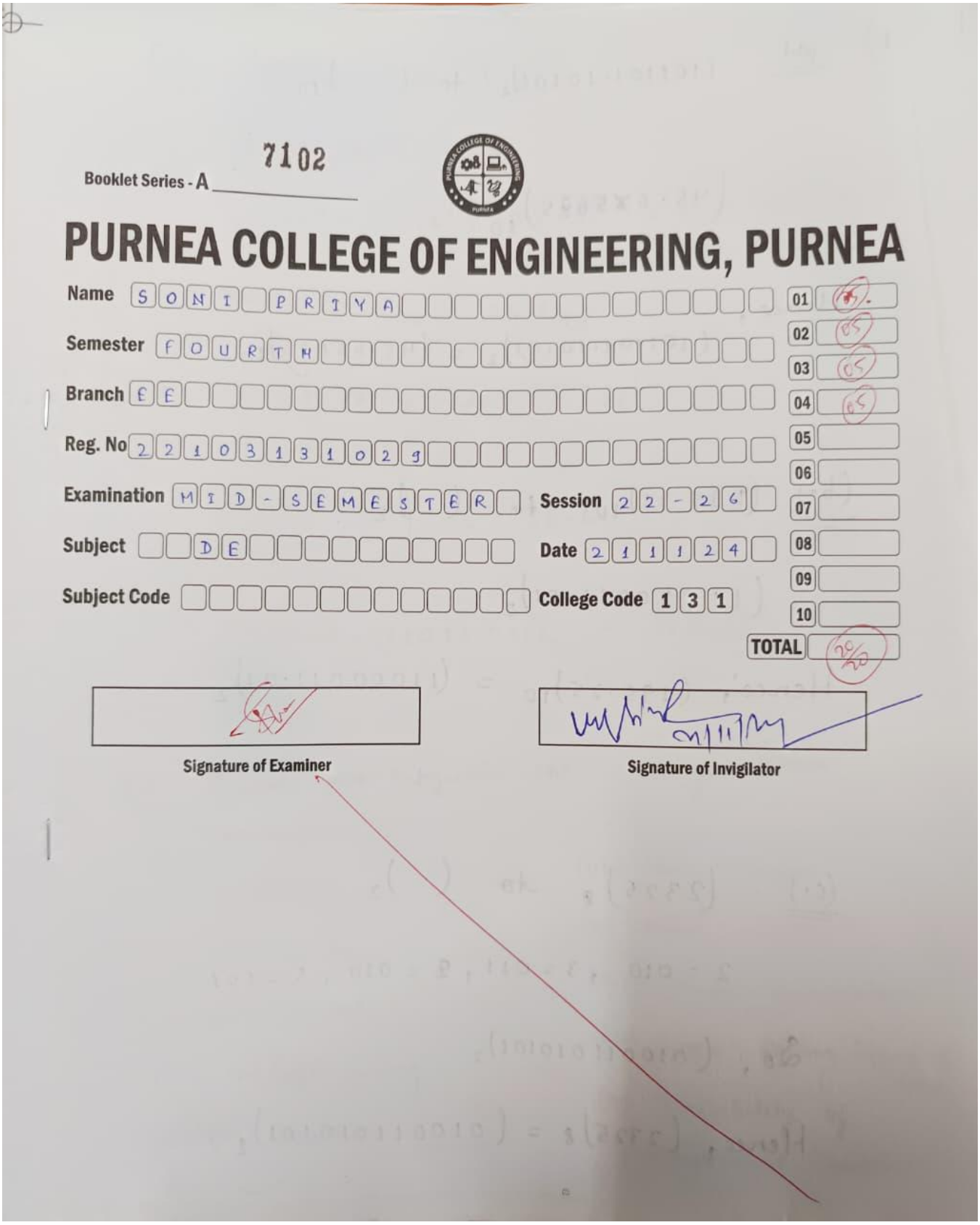
$0.25\times2 = 0.50 \rightarrow 0$

$0.50\times2 = 1.0 \rightarrow 1$

$(11000011.01)_2$

Hence $(195.25)_{10} = (11000011.01)_2$.

Good Student



Booklet Series - A 7102

PURNEA COLLEGE OF ENGINEERING, PURNEA

Name SONI PRIYA

Semester FOURTH

Branch EE

Reg. No 22103131029

Examination MID-SEMESTER Session 22-26

Subject DE Date 21/11/24

Subject Code College Code 131

01	17
02	05
03	05
04	05
05	
06	
07	
08	
09	
10	
TOTAL	20/20

Signature of Examiner

Signature of Invigilator

1.) (a.) $(101101.10101)_2$ to $(\quad)_{10}$

$(45.65625)_{10}$

Hence, $(101101.10101)_2 = (45.65625)_{10}$

(b.) $(195.25)_{10}$ to $(\quad)_2$

$(11000011.01)_2$

Hence, $(195.25)_{10} = (11000011.01)_2$

(c.) $(2325)_8$ to $(\quad)_2$

2 = 010 , 3 = 011, 2 = 010 , 5 = 101

So, $(010011010101)_2$

Hence, $(2325)_8 = (010011010101)_2$

(d.) $(A3B)_{16}$ to $(\quad)_{10}$

A = 10, B = 11, C = 12 ...

then $11 \times 16^0 + 3 \times 16^1 + 10 \times 16^2 = 11 + 48 + 2560$

$= 2619$

Hence, $(A3B)_{16} = (2619)_{10}$

(e.) $(11011.011)_2$ to $(\quad)_{16}$

$\left(\begin{matrix} 11011.011 \\ \leftarrow\ \leftarrow\ \leftarrow \\ 1\ \ B\ \ 6 \end{matrix}\right) = 1B.6$

Hence, $(11011.011)_2 = (1B.6)_{16}$

05

2.) Digital Integrated cht are of various characteristics :-

(i.) Speed
(ii.) Fan in
(iii.) Fan out
(iv.) Logic swing
(v.) Breathe
(vi.) Noise Margin
(vii.) Noise Immunity
(viii.) Power dissipation
(ix.) Logic Swing Figure of Time
(x.) Availability of complement output

(xi.) Power Delay

In detailed explanation :-

(i.) Speed :- Determination of time between the application of input and change in output.

(ii.) Fan in :- Maximum no. of logic gates in inputs without any voltage degradation.

(iii.) Fan out :- No. of inputs without any voltage degradation.

(iv.) Logic Swing :- The difference between two output voltage.

(v.) Breathe :- The various ~~transitions~~ functions of logic gates family.

(vi.) Noise margin :- Its across upto high frequency.

(vii.) Noise immunity :- Boost the frequency, that it can withstand upto high.

(viii.) Power dissipation :- Power as per logic gates.

$P_{dc\,(avg)} = V_{dc} \cdot I_{mean}$

⟶ Product of average current and voltage dissipation, is known as power dissipation.

(ix.) Figure of time :- Product of power dissipation and power delay

(x.) Availability of complement output :- This eliminates the additional inverters.

(xi.) Power Delay :- Change in output to input.

* T_{PLH} :- Going from low to high. (0 to 1)

* T_{PHL} :- Going from high to low. (1 to 0).

3.) (a.)

$AB + A(B+C) + B(B+C)$

$= AB + AB + AC + B + BC$

$= AB + AC + B + BC$

$= AB + AC + B(1+C)$

$= AB + B + AC$

$= B(1+B) + AC = B + AC$

Hence,

$$AB + A(B+C) + B(B+C) = B + AC$$

(b.) $\overline{\overline{A+B\bar{C}} + D(\overline{E+\bar{F}})}$

$= \overline{\bar{A} \cdot \overline{B\bar{C}} + D\bar{E} \cdot \bar{\bar{F}}}$

$= \overline{\bar{A}(\bar{B}+\bar{\bar{C}}) + D\bar{E} \cdot F}$

$= \overline{\bar{A}(\bar{B}+C) + D\bar{E}F}$

$= \overline{\bar{A}(\bar{B}+C)} \cdot \overline{D\bar{E}F}$

$= \left[\bar{\bar{A}} + \overline{(\bar{B}+C)}\right] \cdot \left(\bar{D} + \bar{\bar{E}} + \bar{F}\right)$

$= \left[A + \left(\bar{\bar{B}} \cdot \bar{C}\right)\right] \cdot \left(\bar{D} + E + \bar{F}\right)$

$= \left(A + B\bar{C}\right)\left(\bar{D} + E + \bar{F}\right)$

$= (A+B)(A+\bar{C})\left(\bar{D} + E + \bar{F}\right)$ (05)

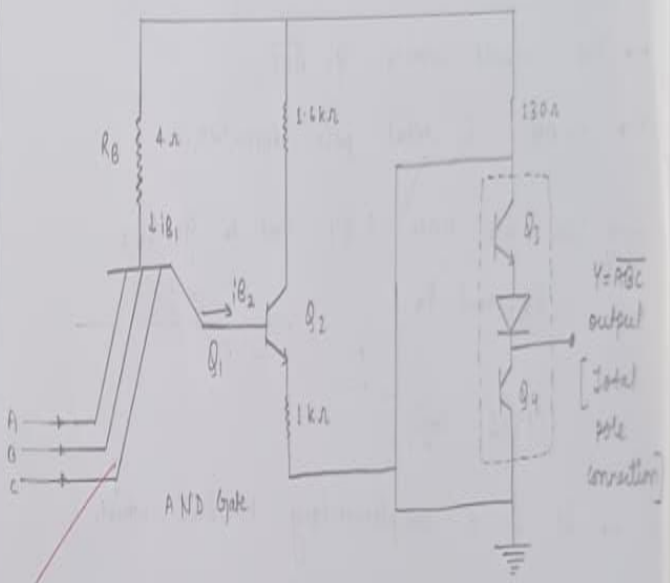
Hence, $\overline{\overline{A+B\bar{C}} + D(\overline{E+\bar{F}})} = (A+B)(A+\bar{C})(\bar{D}+E+\bar{F})$

1.) (a.) TTL circuit

Texas instruments introduced transistor-transistor logic, family of the digital device in 1964.

↦ The basic TTL is NAND gate.

↦ Diagram of 3-input TTL NAND gate is shown below.



Q_3 operates the logic 0 o/p

Q_4 operates the logic 1 o/p

fig:- 3-input TTL NAND gate

Principle of TTL circuit :-

At first, Q_3 is in collector of transistor enters. The Q_4 in emitter of transistor.

→ Q_3 operates the logic 0 output.

→ Q_4 operates the logic 1 output.

In this diagram, there are 4 resistances such as 1.6 kΩ, 1kΩ. are in kΩ and other two are in Ω (4Ω, 130Ω).

→ The result comes $Y = \overline{ABC}$.

→ $Y = \overline{ABC}$ is total pole connection.

→ The are three 4 Q's that is Q_1, Q_2, Q_3, and Q_4.

(b.) CMOS logic

→ It is a complementary MOSFET which is known as CMOS, connected by p-channel and n-channel MOSFET in series which tied together and the output is taken at the common base.

→ CMOS is used in both logic circuit and memory device

→ CMOS is most widely used popular in MSI and LSI, is only possible for logic gates.

→ Also apply for logic representation, simplification, and digital circuit components.

→ In other words, CMOS is one of the best MOSFET.

Remedial Action for Weak Students

1. Teaching Methodologies

- Simplified teaching
- Visual aids
- Peer learning
- Mentoring

2. Outcome of Remedial Classes

- Improved performance
- Better understanding
- Increased confidence

3. Challenges Faced

- Attendance issues
- Time constraints

4. Suggestions for Improvement

- Continuous remedial classes
- Use of technology
- Increased mentoring