UNIT:5 - DATA TRANSFER SCHEMES AND I/O PORTS.

The IO devices connected to a microcomputer system provides an efficient means of communication between the microcomputer system and the outside world. These IO devices are commonly called peripherals and include Keyboards, CRT display, Printerns, hard disk, etc.

Since the characterstic of the IO devices are not compitable with that of the microprocessor, interface hardware circuitry between the microprocessor and I/o devices are necessary.

There are three major types of data transfer between the microcomputer and an IO device. They are as follows.

1) Programmed IO data transfer
2) Interrupt IO data transfer
3) Direct memory access (DMA).

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Programmed IO data transfer: It is of two types:

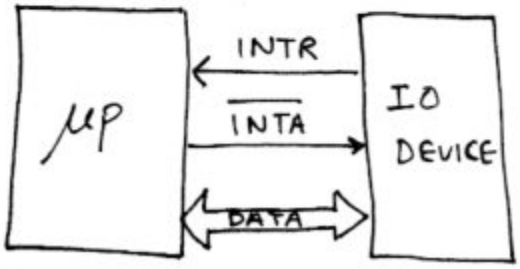
a) Synchronous
b) Asynchronous

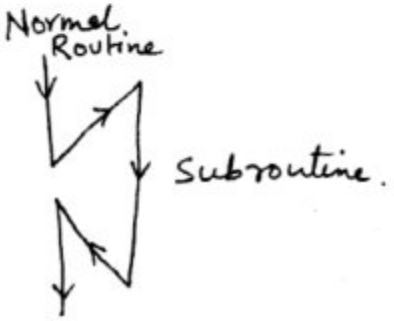
a) Synchronous: When the speed of IO devices is compatible to CPU, Synchronous type of data transfer can be achieved In this mode the status of the device is not checked before undertaking any data transfer, that means, the device is assumed to be ready when the data transfer takes place. This is the simplest scheme and requires minimum hardware/software to implement.

b) Asynchronous: In this mode of data transfer the CPU has to check the status of the IO devices for the availability of the data to be transferred, whether IO device is free to accept the data from the CPU. This mode is used when the speed of the IO device is slower than CPU. This scheme is also known by the name "handshake I/O".

INTERRUPT IO DATA TRANSFER:

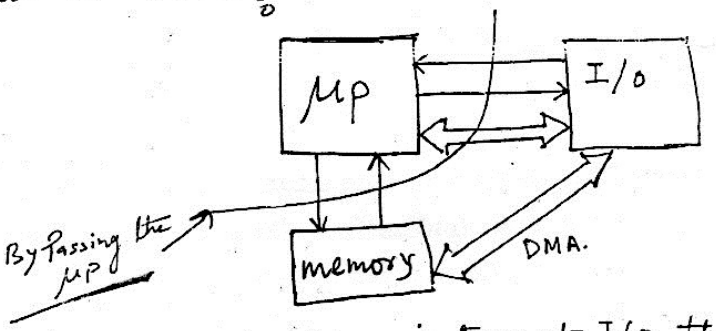
This mode is used for data transfer with slow peripheral and also when the occurence of data is unpredictable in nature. In this method data transfer is achieved by interrupting the microprocessor by the device. When the device is ready for data transfer, it sends an interrupt request signal to the microprocessor, the microprocessor then sends an interrupt acknowledge signal to the IO device indicating that it has received the request and suspends its job after completing its current instruction, it saves the current address and status and execute the ISS (Interrupt service Subroutine).





DIRECT MEMORY ACCESS (DMA)

Q. What is DMA?



Either in Programmed I/O or interrupt I/O, the data transfer between I/O and external memory is via the Accumulator, for voluminous (huge) / large data transfer this method are time consuming and uneconomical even though the I/O devices speed matches with the speed of μP. In such situation it is advisable to provide facilities for transfer of data directly between I/O and the external memory without going through the Accumulator.

DMA is a special type of I/O technique used for high speed data transfer between system memory and Peripherals, by Passing the μP.

Explain the function of HOLD & HLDA Pins of 8085

HOLD :- This is Active high Signal from DMA controller to 8085 µP. This Signal indicates that the DMA controller is requesting the use of the address and data bus of 8085.

HLDA : This is Active high Signal from µP to the DMA controller After receiving the HOLD signal from the DMA controller µP releases its address and data bus and generates HLDA for the DMA controller.

Explain the following term / Signal :-

SLAVE MODE & MASTER MODE :- During the DMA Process, Initially the DMA chip (8237 or 8257) is slave and 8085 master, 8085 loads control words, count value to DMA chip, then µP releases HLDA, then it give the control of all data bus to DMA and now the DMA chip acts as a Master, and now the DMA chip will access the data bus, after end of Programme it sends Signal to µP and the order is reversed.

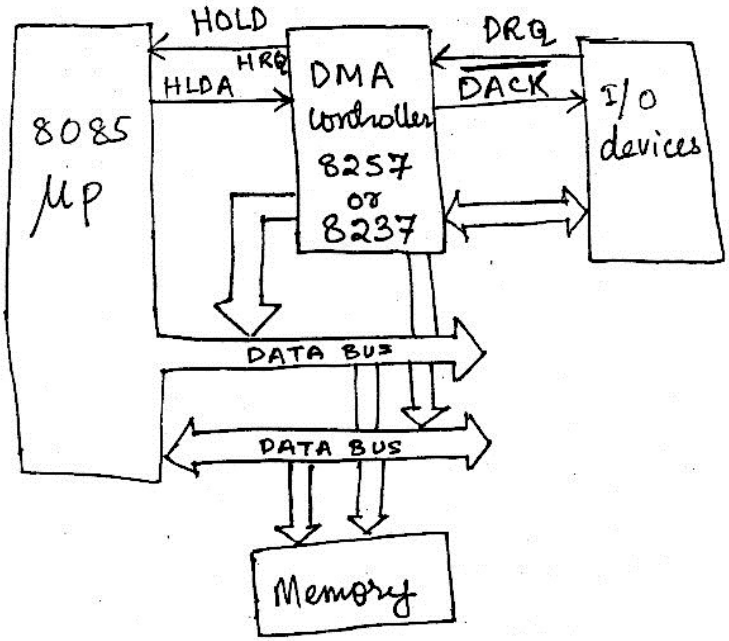
$\overline{\text{DACK}}$: Direct memory access acknowledge.

HRQ :- Hold Request.

DRQ :- Direct memory excess request.

It is sent by I/O to DMA controller, then the DMA controller Sends Signal HRQ which is connected to the HOLD Pin of 8085, after receiving HOLD µP Sends HLDA, this means µP releases the control of data bus and now the DMA controller Sends $\overline{\text{DACK}}$ to I/O devices, now the I/O device starts to transfer data from the memory.

Discuss the steps for data transfer process between a floppy disk and R/W memory of 8085 System using DMA.



The Process of data transfer between the System memory and Peripheral under DMA controller can be classified between two mode.

1 SLAVE MODE :- In this mode the DMA controller is treated as a Peripheral using following steps: (a) The MPU selects DMA controller through chip select (CS) line

(b) The MPU writes the control word in channel register and command / status register by using control signal $\overline{IOW}$ and $\overline{IOR}$.

2 MASTER MODE : After the Initialization, the 8237 in master mode keeps checking for a DMA request and the steps in data transfer can be listed as follows:

(a) when the Peripheral is ready for data transfer it sends an active high signal to DRQ line of 8257.

(b) After receiving the DRQ signal 8257 generates an active high HRQ (Hold Request) signal which is connected to HOLD Pin of 8085.

(c) After receiving HOLD signal the μP releases its Buses and sends the HLDA (Hold acknowledge signal) to 8257.

(d) After receiving the HLDA signal from μP the DMA controller sends $\overline{DACK}$ to the Peripheral.

(e) Peripheral Places it's data on the buses and starts data transfer between Peripheral and System memory.

(f) At the end of data transfer the DMA controller generates $\overline{EOP}$ (end of process) to inform the Peripheral that data transfer is complete.

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