Data types :-

→ Each data object has a type associated with it. The type defines the set of values that the object can have and the set of operations that are allowed on it. The notion of type is key to VHDL since it is a strongly typed language that requires each object to be of certain type.

1. Data types defined in the standard package

→ VHDL has several predefined types in the standard package. To use this package one has to include the following clause :-

```
Library std, work;
use std.standard.all;
```

types defined in Package Standard of std library :-

Type	Range of values	Example
bit	'0', '1'	signal A : bit := 1;
bit_vector	an array of each element of type bit	signal INBUS : bit_vector (7 downto 0);
boolean	FALSE, TRUE	variable TEST : Boolean := FALSE;
character	any legal VHDL character, printable characters must be placed between single quotes (eg : '#')	variable VAL : character := '$';

Type	Range of values	Example
integer	range is implementation dependent but includes at least $\{-(2^{31}-1)$ to $+(2^{31}-1)$	constant CONST1 : integer := 129;
natural	integer starting with 0 up to the max specified in the implementation	variable var1 : natural := 2;
positive	integer starting with 1 up to the max specified in the implementation	variable var2 : positive := 2;
security_level	note, warning, error, failure.	
String	array of which each element is of the type character	variable var1 : string (1 to 12) := " $#@%. ";

2. User-defined Types :-

→ we can introduce new types by using the type declaration, which names the type and specifies its value range.

type identifier is type-definition ;

(a) integer types :-

eg:- type small_int is range 0 to 1024;

type my_word_length is range 31 downto 0;

Subtype data_word is my_world_length range 7 downto 0;

↓

A subtype is a subset of a previously defined type.
Here, in this example data_word is a subtype of my_word_length, of which range is restricted from 7 to 0.

(b) Floating-point types:-

eg:-
```
type cmos_level is range 0.0 to 3.3;
type pmos_level is range -5.0 to 0.0;
Subtype cmos_level_Vol is cmos_level range 0.0 to 1.8;
```

(c) Physical types:-

It includes a units identifier as follows:-

eg:-
```
type conductance is range 0 to 2E-9 units
        mho;
        mmho = 1E-3 mho;
        umho = 1E-6 mho;
        nmho = 1E-9 mho;
    end units conductance;
```

→ Here, a space must be left before the unit name.

3. Enumerated types:-

- consists of lists of character literals or identifiers

type type_name is (identifier list or character literal);

eg:-
```
type my_3values is ('0', '1', 'Z')
type hex_digit is ('0', '1', '2', '3', '4', '5', '6', '7', '8',
                   '9', 'A', 'B', 'C', 'D', 'E', 'F');
```

→ An example of an enumerated type that has been defined in the std_logic_1164 package is the std_ulogic type, defined as follows:-

```
type std_ulogic is ('U', -- uninitialized
                    'X', -- forcing unknown
                    '0', -- forcing 0
                    '1', -- forcing 1
                    'Z', -- high impedance
                    'W', -- weak unknown
                    'L', -- weak 0
                    'H', -- weak 1
                    '-', -- don't care
                    );
```

In order to use this type one has to include the clause before each entity declaration

```
Library ieee;
use ieee.std_logic_1164.all;
```