Synchronous (Parallel) Counter

Asynchronous (ripple) counter is the simplest type of binary counter as it requires less hardware. But its speed of operation is low because the propagation delay time of all flip-flop is cumulative and the total Settling time is the product of the total number of flip-flops and the propagation delay of a single flip-flop.

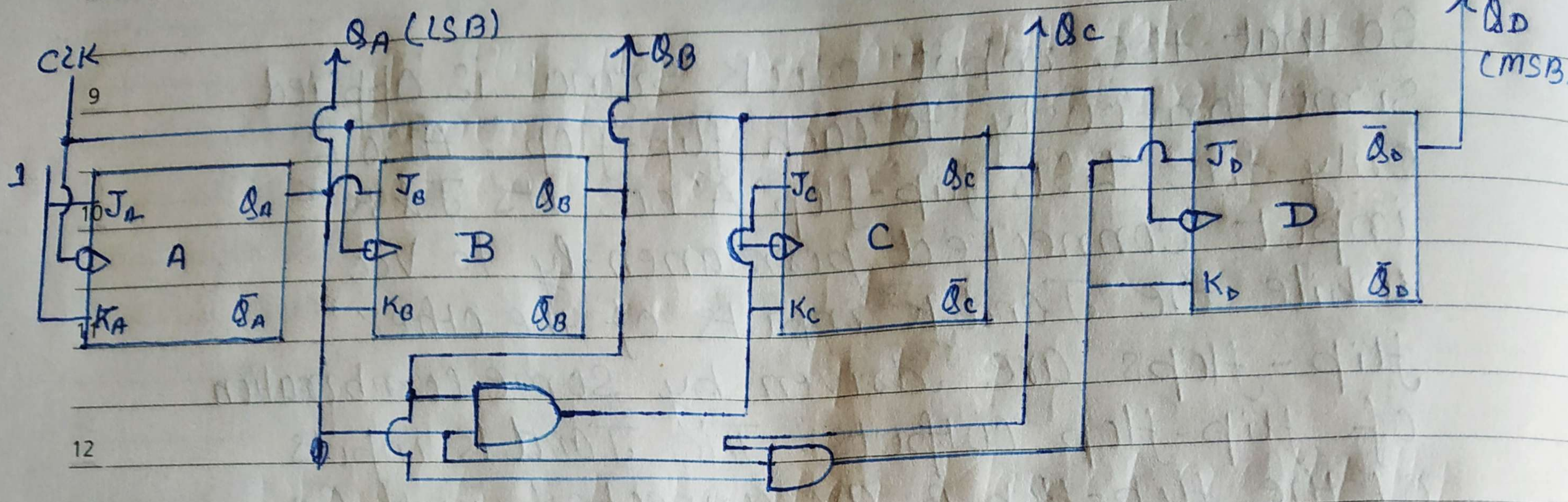
Another problem encountered with ripple Counter is the glitches at the decoding gate output. These problems can be eliminated by applying clock pulses to all the flip-flop simultaneously, which is done in a synchronous Counter.

The Speed of operation in a synchronous counter is limited by the propagation delay of control gating and a flip-flop.

DAY Given below is diagram of a 4-bit (MOD-16) Synchronous counter with parallel Carry. In this counter, the clock input of all the flip-flop are connected together

So that the input clock signal is applied simultaneously to each flip-flop. Also, only the LSB flip-flop 'A' has its J & K input connected permanently to Vcc while the J and K inputs of the other flip-flops are driven by some combination of flip-flop outputs. The J and K inputs of the flip-flop B are connected with Q_A output of flip-flop A; the J and K inputs of flip-flop C are connected with AND operated output of Q_A and Q_B; Similarly the J and K inputs of D flip-flop are connected with AND operated output of Q_A, Q_B and Q_C.

Flip-flop A changes its state with the occurrence of negative transition at each clock-pulse. The flip-flop B changes its state when $Q_A = 1$ and when there is negative transition at clock input. Flip-flop C changes its state when $Q_A = Q_B = 1$ and when there is negative transition at clock input. Similarly, D flip-flop changes its state when $Q_A = Q_B = Q_C = 1$ and when there is negative transition at clock input.



CLK	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
16	0	0	0	0

In a parallel counter, all the flip-flop change their states simultaneously i.e they are all synchronised with the negative transition of the input clock signal. Thus, unlike asynchronous counter where the total propagation delay is cumulative, the total settling or response time of a synchronous Counter is given as the time taken by one flip-flop to toggle plus the time for the new logic levels to propagate through a single AND gate to reach the J & K inputs of the following flip-flop.

Total delay = Propagation delay of one flip-flop + Propagation delay of AND gate

The total delay will be the same irrespective of the number of flip-flops present in the counter, and it will normally be much lower than that of an asynchronous Counter with the same number of flip-flops. Therefore, the speed of operation of Synchronous counter is limited only by the propagation delay of a

single flip-flop and an AND gate. The maximum frequency of operation of synchronous counter is given by

$$f_{max} = \frac{1}{t_p + t_g}$$

where, t_p = propagation delay of one flip-flop
t_g = propagation delay of one AND gate

Because of common clocking of all the flip-flops, glitches can be avoided completely in synchronous counters.

However, the synchronous counter has more complex circuitry than an asynchronous counter.