COUNTERS

A Counter, by function is a sequential circuit consisting a set of flip-flops connected in a suitable manner to count the sequence of the input pulses presented to it in digital form. Counters can be broadly classified as

i) Asynchronous and Synchronous Counter
ii) Single and multi-mode counter
iii) Modulus counters.

Asynchronous Counter :- It can be constructed using minimum hardware, each flip-flop is triggered by the output from the previous flip-flop which limits its speed of operation.

Synchronous Counter :- In this kind of counter, the clock-pulses are applied simultaneously to all the flip-flops. Hence settling time of counter is equal to propagation delay of a single flip-flop.

Single mode counter operate in a single mode i.e it counts either in the UP mode or in the DOWN mode.

Multimode counter operate in both UP and DOWN modes

Modulus counters are defined based on the number of states they are capable of counting.

Counters are fundamental components of digital system. Digital counters find wide application like pulse counting, frequency division, time measurement and control and timing operation.

Asynchronous or Ripple or Serial Counter

In this counter, clock pulse is applied to the first flip-flop i.e to the least significant bit stage of the counter and the successive flip-flop is triggered by the output of the previous flip-flop and thus the counter has a cumulative settling time.

The first stage of the counter switches first, on the application of a clock pulse. This change in state of first flip-flop acts as clock input to the second stage flip-flop. Similarly change in state of second stage flip-flop acts as clock input to

third stage flip-flop. The successive stages changes their state in turn causing a ripple-through effect of the count pulses. As the trigger move through the flip-flop like a ripple, it is called a ripple counter.

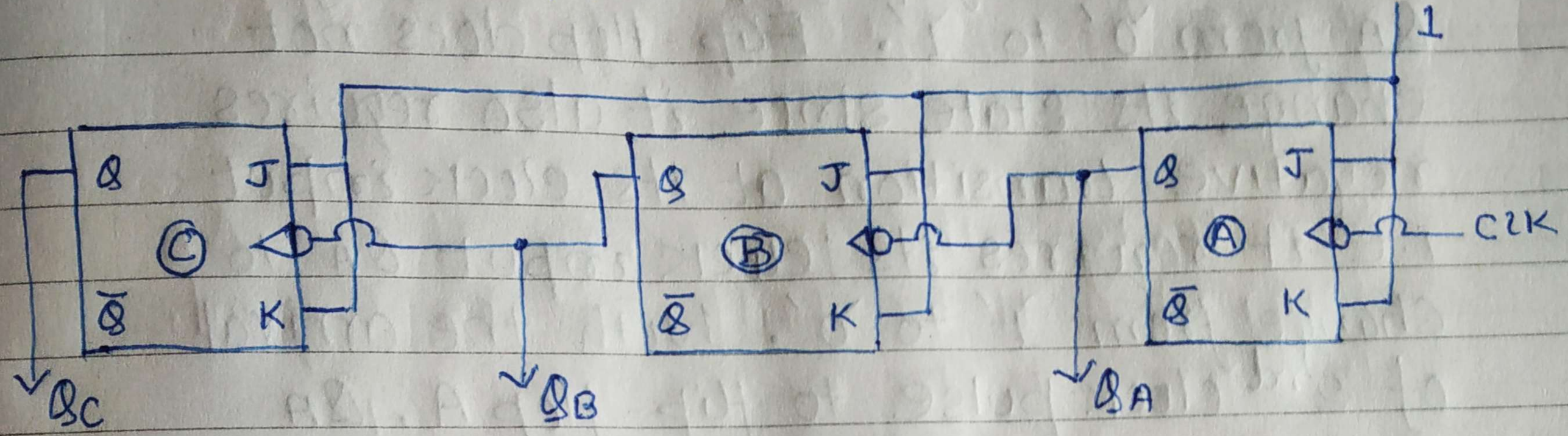


Diagram shows 3-bit binary ripple counter. It is constructed using J-K flip flop. The least Significant flip-flop 'A' receives clock signal. The output of flip-flop A drives flip-flop B, the output of flip-flop B drives flip-flop C and so on.

The flip-flop is negative edge trigged i.e flip-flop will change its state only when clock or output of previous flip-flop changes from '1' to '0'.

All the J and K inputs are connected to '1', which means that each flip-flop toggles on the negative edge of its clock input.

Operation

Consider initially all flip-flops are in reset state i.e $Q_C=0$, $Q_B=0$ & $Q_A=0$. A negative transition (1 to 0) in clock input drives flip-flop A to change Q_A from '0' to '1'. Flip-flop does not change its state since it also requires negative transition at its clock input i.e it requires its clock input Q_A to change from '1' to '0'. With the arrival of 2nd clock pulse to flip-flop A, Q_A goes from '1' to '0'. This change of state creates the negative going edge needed to trigger flip-flop B, and thus Q_B goes from '0' to '1'.

Truth table of 3-bit ripple counter can be given as

	Q_C	Q_B	Q_A	CLK	
Initally Reset →	0	0	0	0	
	0	0	1	1	← 1st (-)ve edge of clock
	0	1	0	2	
	0	1	1	3	
	1	0	0	4	
	1	0	1	5	
	1	1	0	6	
	1	1	1	7	
	0	0	0	8	

An n-bit binary counter repeats the counting sequence for every 2^n (n = number of flip-flops) clock pulses and has discrete states from 0 to $2^n - 1$.

The Counter in diagram has 8 different states. Thus, it is a MOD-8 ripple Counter. The MOD-number (or the Modulus) of a counter is the total number of states it sequences through in each complete cycle.

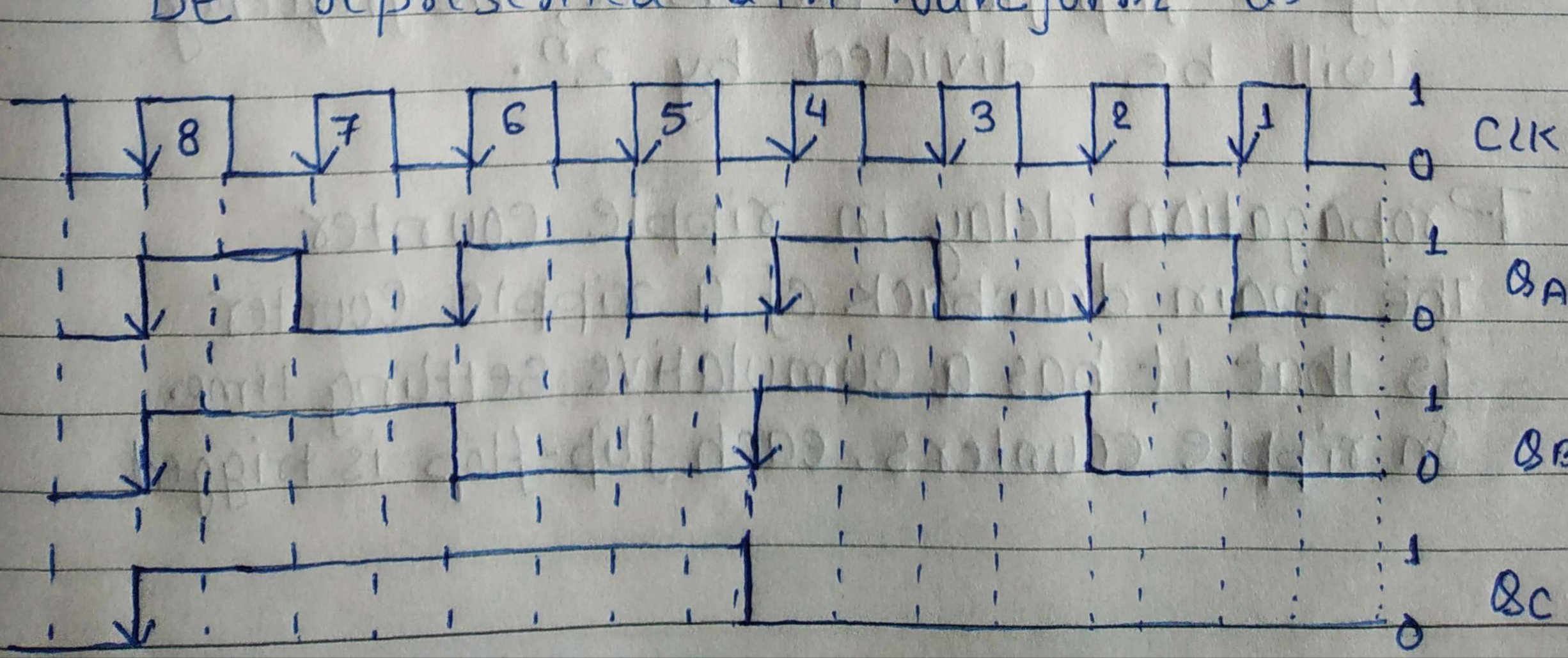
$$\text{MOD number} = 2^n$$

where n = no. of flip-flop.

The maximum binary number counted by the counter is $2^n - 1$. Thus, a 3-flip flop counter will count as high as

$$(111)_2 = 2^3 - 1 = (7)_{10}$$

The truth table of 3-bit flip flop can also be represented in waveform as.



frequency division

Look at the waveform of truth table.
Let, the input clock frequency be f_{CLK}.
We find that, two clock pulses are required for a single pulse at Q_A.
Hence the frequency of Q_A will be $f_{CLK}/2$.

Similarly, the frequency of the Q_B signal will be half of Q_A signal.
Therefore, its frequency is $f_{CLK}/4$.

Similarly the frequency of Q_C will be $f_{CLK}/8$.

Thus, the circuit can be used to divide or scale down the input frequency. Such a circuit are called frequency divider.

If n-flip-flops are used, the frequency will be divided by 2^n.

Propagation delay in ripple counter

The main drawback of a ripple counter is that it has a cumulative settling time. In ripple counters, each flip-flop is trigged

by the transition at the output of the preceding flip-flop. Because of the inherent propagation delay time (t_{pd}) of each flip-flop, the first flip-flop will not respond for a period of t_{pd} even after receiving a clock pulse. Similarly, the second flip-flop will not respond for a period of $2.t_{pd}$ after the input clock pulse occurs. Hence, the n^{th} flip-flop cannot change states for a period of $n \times t_{pd}$ even after the Clock pulse occurs.

Therefore, to allow all the flip-flop in a n-bit counter to change states in response to a clock, the period of the clock (T_{clock}) should be

$$T_{clock} \geq n \times t_{pd}$$

So, the maximum clock frequency that can be applied in an n-bit asynchronous counter is

$$f_{max} = \frac{1}{n \times t_{pd}}$$

As the number of flip-flop in ripple counter increases, the total delay will increase and f_{max} will become lower.