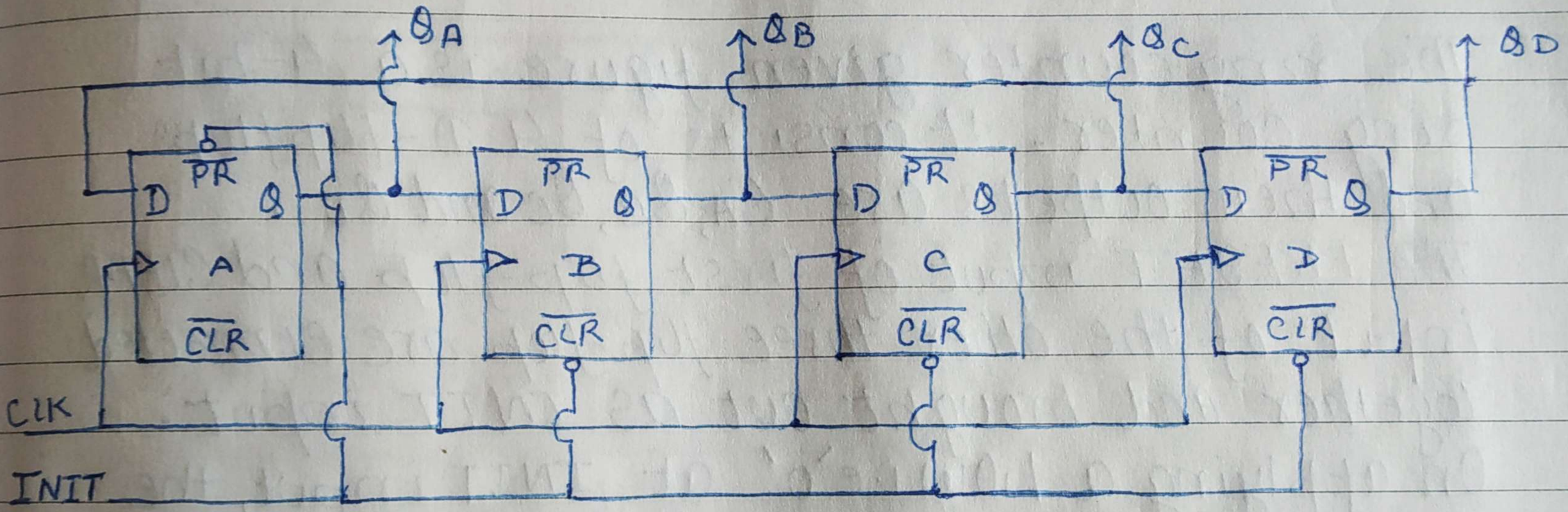
Shift Register Counters

Shift registers can be arranged to form several types of counters. All shift-register counter uses feedback, whereby the output of the last flip-flop in the shift register is connected back to the first flip-flop.

Based on the type of feedback connection, the shift register counters are classified as

i) Standard ring or ring Counter
ii) twisted ring or Jhonson or Shift Counter.

Ring Counter :- In a ring counter, the true output (Q) of the last flip-flop in a shift register is connected back to the serial input of the first flip-flop, and also only one flip-flop is set at any particular time while all others are cleared. Since a single '1' in the register is made to circulate around the register as long as clock pulse are applied, it is called a ring counter.



4-bit ring counter using D-flipflop

Before discussing the operation of ring Counter, we should know about the function of special control inputs of flip-flops PRESET and CLEAR.

If PRESET is enabled i.e PR = 1, then flip-flop will be SET i.e Q = '1', regardless of present state and input at D.

If CLEAR is enabled i.e CLR = '1', then flip-flop will reset i.e Q = '0', regardless of present state and inputs at D.

The PRESET and CLEAR inputs used in ring counter given in figure are low enable i.e

when $\overline{PR} = 0$, then $Q = 1$

$\overline{CLR} = 0$, $Q = 0$

The ring counter given figure is a 4-bit ring counter. It consists of 4 D-flipflops and their outputs are Q_A, Q_B, Q_C and Q_D. The PRESET input of first flip-flop and CLEAR input of the other three flip-flop are connected together and brought out as INIT input. On applying a LOW i.e '0' at INIT input, the first flip-flop is SET to 1 and the other three flip-flop are cleared to 0. So output will be

$Q_A = 1$, $Q_B = 0$, $Q_C = 0$ and $Q_D = 0$

So, input at flip-flop would be

$D_A = 0$, $D_B = 1$, $D_C = 0$ and $D_D = 0$

Set INIT = '1', and then give CLK = 1

After 1st clock pulse

$Q_A = 0$, $Q_B = 1$, $Q_C = 0$ and $Q_D = 0$

$D_A = 0$, $D_B = 0$, $D_C = 1$, and $D_D = 0$

After 2nd clock pulse

$Q_A = 0$, $Q_B = 0$, $Q_C = 1$, and $Q_D = 0$

$D_A = 0$, $D_B = 0$, $D_C = 0$ and $D_D = 1$

After 3rd clock pulse

$Q_A = 0$, $Q_B = 0$, $Q_C = 0$ and $Q_D = 1$

$D_A = 1$, $D_B = 0$, $D_C = 0$ and $D_D = 0$

After 4th clock pulse

$Q_A = 1$, $Q_B = 0$, $Q_C = 0$ and $Q_D = 0$

INIT	CLK	Q_A	Q_B	Q_C	Q_D
0	X	1	0	0	0
1	1	0	1	0	0
1	1	0	0	1	0
1	1	0	0	0	1
1	1	1	0	0	0

Truth Table for 4-bit ring counter

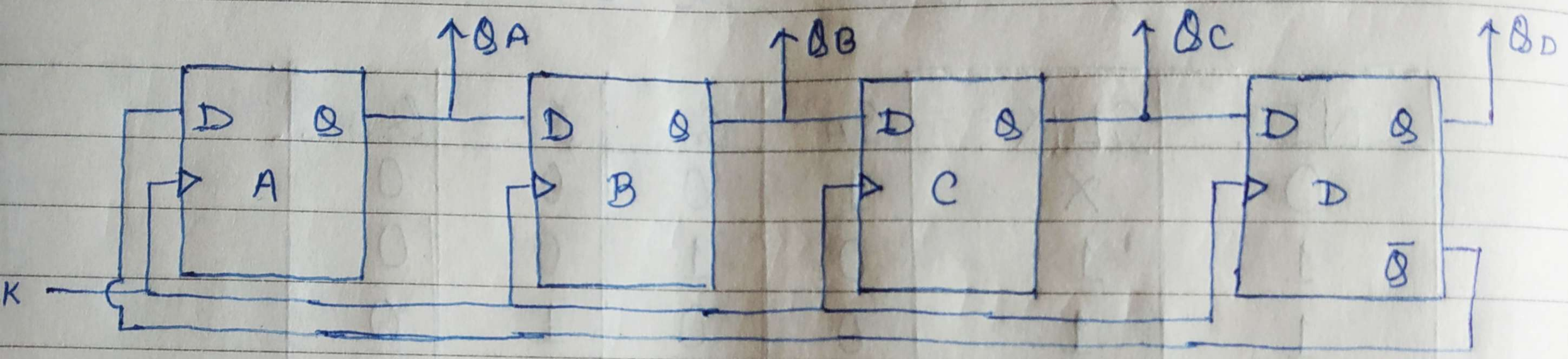
Thus 1 is shifted or circulated around the register as long as clock pulse are applied.

The ring counter has only 4-valid States i.e 1000, 0100, 0010, 0001.

The ring counter can enter invalid States due to noise or any other condition without returning to the main counting sequence.

Shift Counter or Johnson Counter

The Shift or twisted-ring counter is constructed similar to a standard ring counter except that the inverted output of the last flip-flop is connected to the input of the first flip-flop. This Counter is known as the Johnson counter.



4-bit Shift Counter or Johnson Counter

A 4-bit Johnson Counter using D-flip-flop is given in figure. The output of each flip-flop (Q) is connected to the D-input of the next stage. However, the inverted output of the last flip-flop i.e $\bar{Q}_D$ is connected to the D input of the first flip-flop.

Assuming that initially ~~all~~ the counter is reset to 0 i.e $Q_A Q_B Q_C Q_D = 0000$

$D_B = D_C = D_D = 0$, but $D_A = 1$

Applying clock pulse, CLK = 1, truth table ~~Cobe~~ can be depicted as

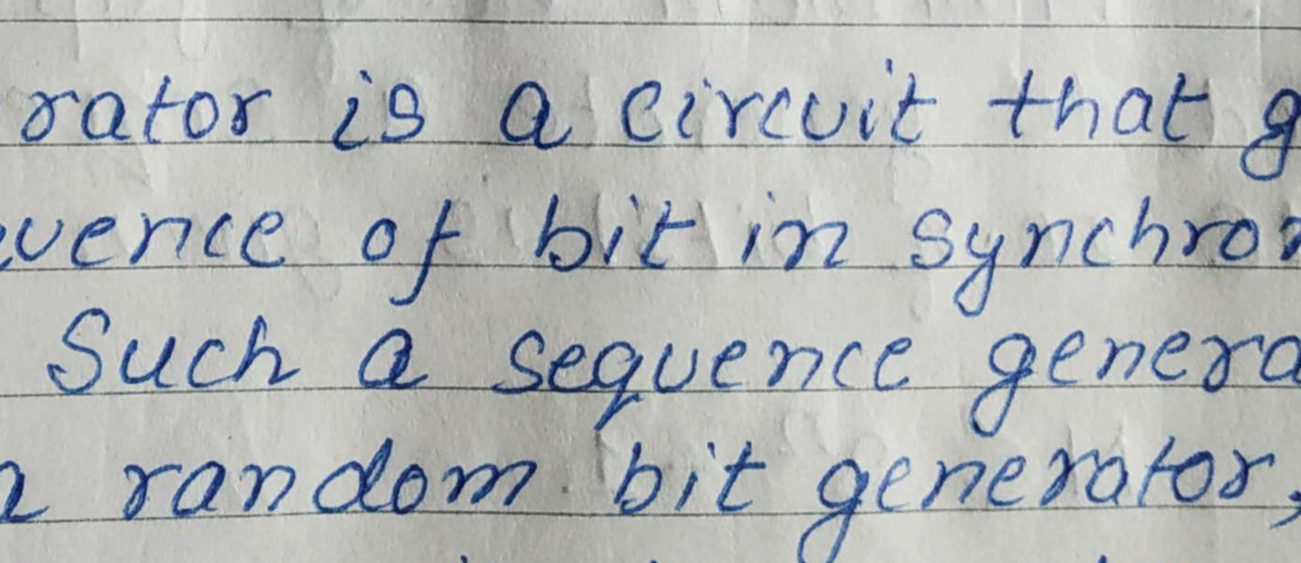
Clk	Q_A	Q_B	Q_C	Q_D	$\overline{Q_D}$
0	0	0	0	0	1
1	1	0	0	0	1
2	1	1	0	0	1
3	1	1	1	0	1
4	1	1	1	1	0
5	0	1	1	1	0
6	0	0	1	1	0
7	0	0	0	1	0
8	0	0	0	0	1

Truth table of 4-bit Johson Counter

We see that 4-bit Johnson Counter has 8 valid States given in its truth table.

Sequence Generator

Sequence generator is a circuit that generates a desired sequence of bit in synchronization with a clock. Such a sequence generator can be used as a random bit generator, code generator and prescribed generator. The block diagram of a sequence generator is given below



The sequence generator can be constructed using shift register and next state decoder. The output of the next state decoder (z) is a function of Q_{n-1}, ... Q_1 & Q_0 and is connected to the serial input of the shift register.

This sequence generator is similar to ring counter / shift counter in which Q_0 & $\overline{Q_0}$ is connected to the serial input of the shift register and hence they are special case of sequence generators.

Procedure to design a sequence generator to generate 11001.

Step 1 :- Minimum no. of flip-flop (n) required to generate a sequence length N (ie no. of bits) is given by

$$N \leq 2^n - 1$$

For the given problem $N = 5$, so, the minimum value n, that will satisfy the above inequality is $n = 3$ i.e three flip-flops are required to generate the given sequence.

Step-2 :- State table for 5 bit (11001) Sequence generator.

	CLK	Flip-Flop output Q_2	Q_1	Q_0	Serial Z Input
C_0	1	1	1	0	1
C_2	2	1	1	1	0
C_3	3	0	1	1	0
C_4	4	0	0	1	1
C_5	5	1	0	0	1

The given sequence (11001) is listed under Q_2 and the sequence under Q_1 and Q_0 are the same sequence delayed by one and two clock pulse respectively as indicated by arrow marks.

It is observed that all the 5 states are distinct i.e $C_1 \neq C_2 \neq C_3 \neq C_4 \neq C_5$. ($C_0 = Q_2 Q_1 Q_0$), hence three flip-flops are sufficient to implement the sequence generator.

If any of the states i.e C_1, C_2, C_3, C_4 or C_5 would have been equal to each other, we had to use one more flip-flop.

The last Column gives the Serial input required at the shift

register (i.e D_2 of MSB flip-flop), assuming D flip-flop are used and considering the output Q_2.

Step 3 :- K-Map for the serial input (Z)

Q_0 \ Q_2Q_1	00	01	11	10
0	d	d	1	1
1	1	0	0	d

$$Z = \overline{Q}_0 + \overline{Q}_1$$

From, State table, we simplify for Z i.e serial input

Step 4 :- Drawing logic diagram using simplified expression for Z.