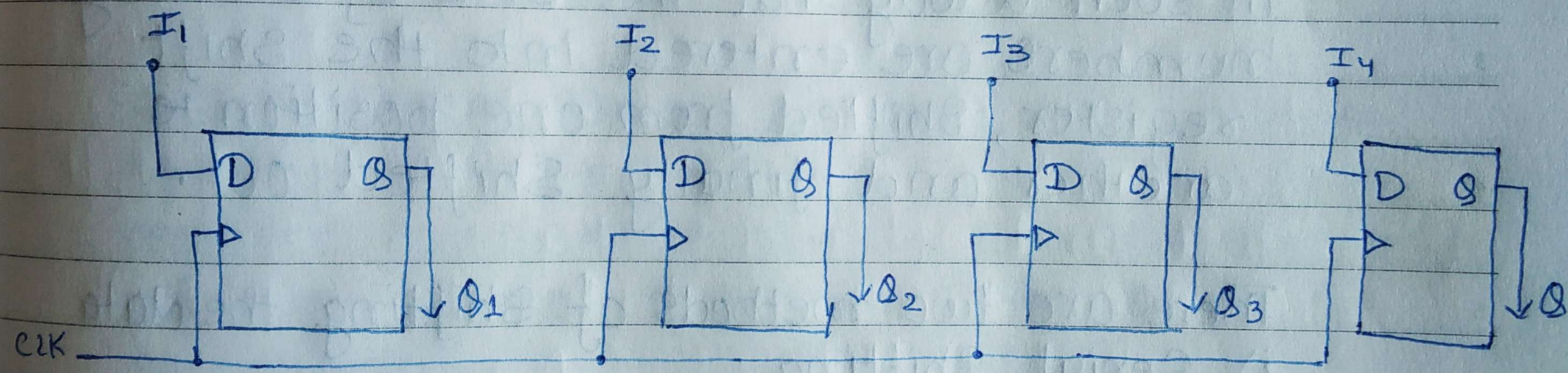
Registers

A register is a group of flip-flop suitable for storing binary information. Each flip-flop is a binary cell capable of storing one bit of information. An n-bit register has a group of n flip-flop and is capable of storing any binary information containing n bits. The register is mainly used for storing and shifting binary data entered into it from an external source.



4-bit register

A simple register using D-flip-flop is shown in figure above. The register has a common clock-pulse input. This clock pulse input enable all flip-flop, so that the information available at the four inputs I_1, I_2, I_3 & I_4 can be transferred into the 4-bit register. The four output Q_1, Q_2, Q_3 & Q_4 can be read to obtain the information presently stored in the register.

Shift Registers :- A registers that is used to store binary information is known as a memory register. A register capable of shifting binary information either to the right or to the left is called a Shift register.

The Shift register permits the Stored data to move from a particular location to Some other location within the register.

In a Shift register, the flip-flop are connected in such a way that the bits of a binary numbers are entered into the shift register, Shifted from one position to another and finally Shifted out.

There are two methods of Shifting the data
i) Serial Shifting
ii) Parallel Shifting

i) Serial Shifting :- This method Shifts one bit at a time for each clock pulse in a Serial fashion, beginning with either MSB or the LSB.

ii) Parallel Shifting :- In this method all data (Input and output) get Shifted Simul-

taneously during a single clock pulse. This method is much faster than the serial shifting method.

Shift registers are classified into the following four types based on how binary information is entered or shifted out

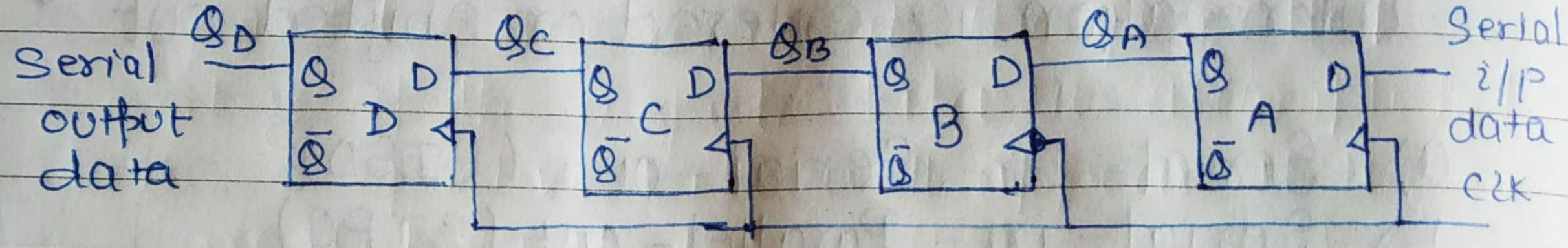
a) Serial-in-Serial-out (SISO)
b) Serial-in-Parallel-out (SIPO)
c) Parallel in-Parallel-out (PIPO)
d) Parallel-in-Serial-out (PISO)

Shift Registers can be designed using discrete flip-flop (S-R, J-K and D-type). An n-bit Shift register consists of n-flip-flop and the required gates to control the Shift operation.

Shift registers are used in digital systems for temporary storage of information, data manipulation and transferring. In addition, they are used in Counting circuits, such as Simple counters, variable modulo counters, Up/Down counters and Increment counters.

a) Serial-in-Serial-out Shift Register

This type of shift register accepts data serially, i.e one bit at a time on a single input line. It produces the stored information on its single output also in serial form.

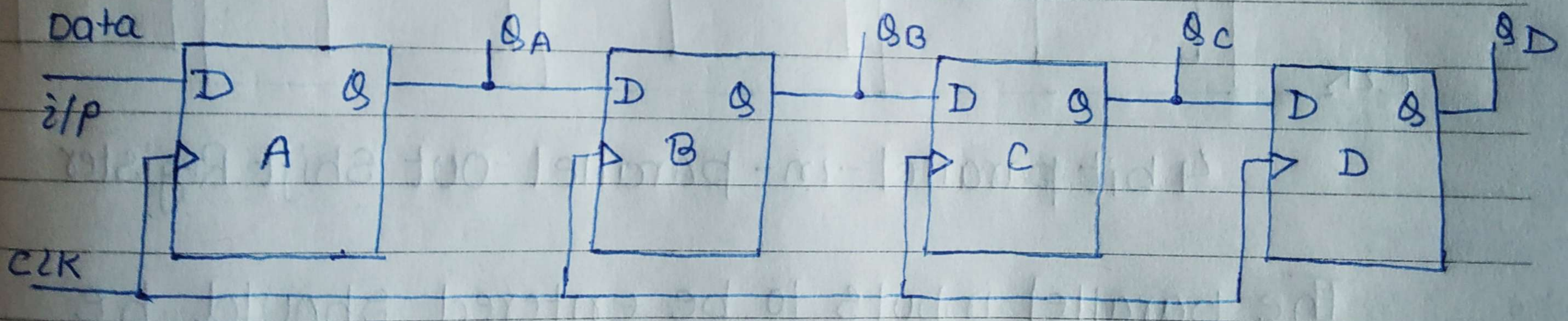


A SISO register is shown in figure. It is implemented using D-flip flop. The input data is provided to rightmost D-flip-flop. With each clock pulse, the data at the input of D-flip flop name 'A' will shift left and after 4 clock pulses, the data will be available at output of 4th D-flip-flop i.e at Q_D.

Let us consider that all stages are reset and a steady logical '1' is applied at the serial input line connected to stage A.

Shift Pulse	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	1
3	0	1	1	1
4	1	1	1	1

b) Serial-in-parallel-out Shift Register :- It consist of one serial input and output are taken from all the flip-flops parallel. In this register, data is shifted in serially but shifted out in parallel. In order to shift the data out in parallel, it is necessary to have all the data available at the output at the same time. Once the data is stored, each bit appears on its respective output line and all the bits are available simultaneously, rather than on a bit-by-bit basis as with the serial output. It is also known as serial to parallel converter.



4-bit Serial-in-parallel-out shift register

Suppose that given serial data is 1011, & we want this data to be available in parallel form. Let us consider that initially all stages are reset.

CLK pulse	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	0	1	1	0
4	1	0	1	1

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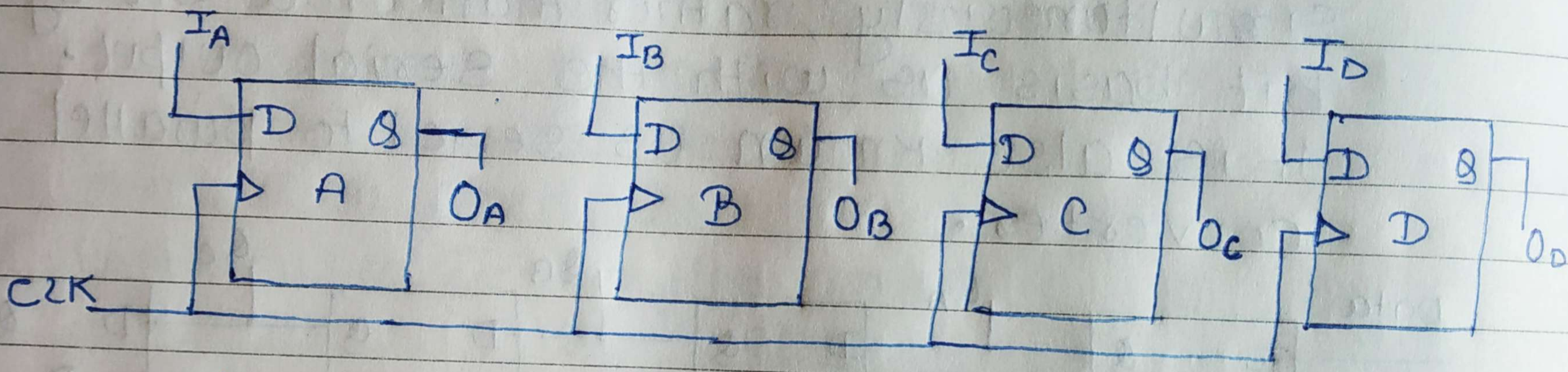
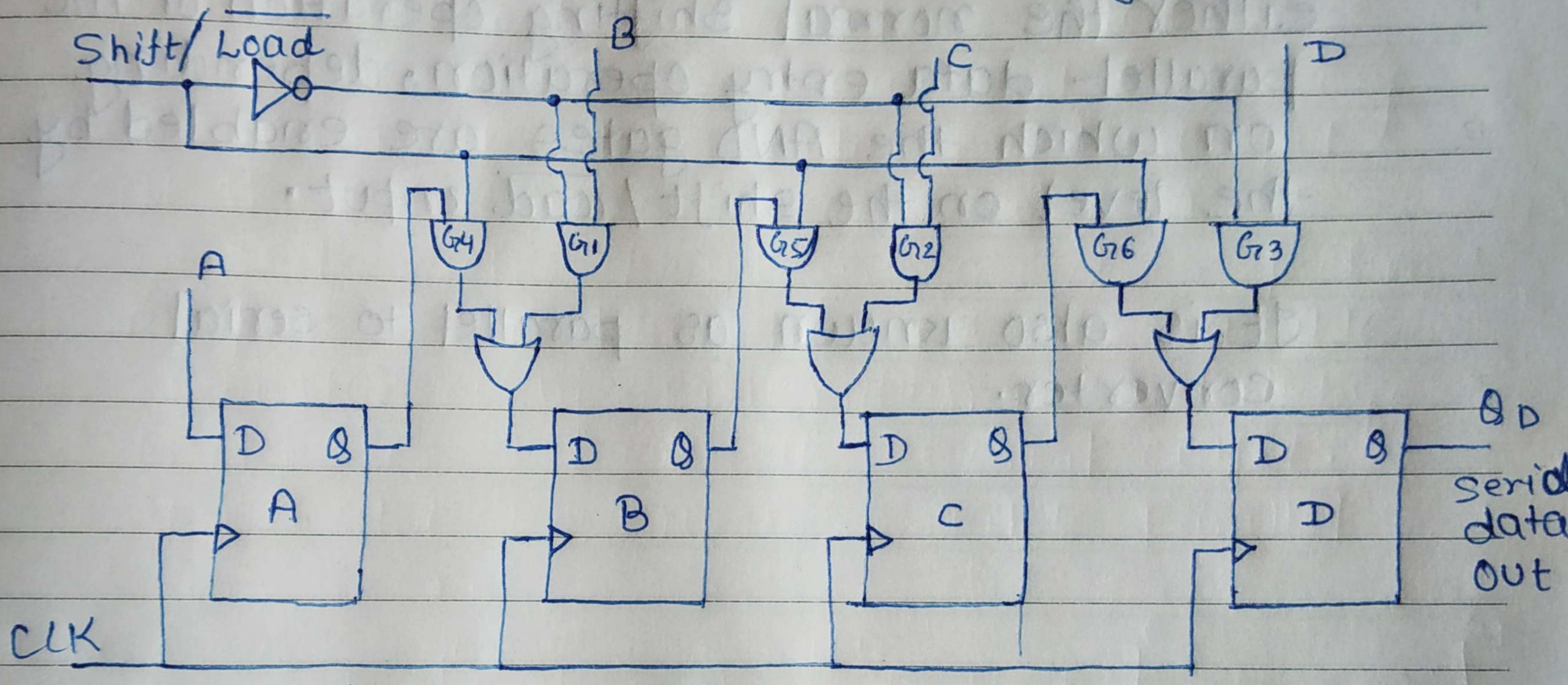
C) Parallel-in-parallel-out Register :- In this type of register, data inputs can be shifted either in or out of the register in parallel. In this register, there is no interconnection between sucessive flip-flop since no serial shifting is required. The moment the parallel entry of the input data is accomplished, the respective bits will appear at the parallel outputs.



4 bit parallel-in-parallel-out Shift Register

The parallel inputs to be entered should be applied at I_A, I_B, I_C, and I_D which are directly connected to delay (D) inputs of respective flip-flops. Now on applying a clock pulse, these inputs are entered into the register and are immediately available at the output O_A, O_B, O_C and O_D.

d) Parallel-in-Serial-Out Shift Register :- In this type of register data is are entered simultaneously into their respective flip-flop and are shifted out serially.



4-bit parallel-in-Serial out Shift register

A, B, C and D are the four parallel data-input lines. Shift/$\overline{\text{Load}}$ is a control input that allows the four bits of data to enter into the register in parallel or shift the data in serial.

When Shift/$\overline{\text{Load}}$ is low, AND gates G1, G2 and G3 are enabled, allowing the data at parallel input B, C and D to the D input of its respective flip-flop. The A input is directly connected to the D input of the first flip-flop.

When Shift/$\overline{\text{Load}}$ is high, AND gate G_1, G_2 and G_3 are disabled and G_4, G_5 and G_6 are enabled, allowing the data bits to shift right from one stage to the next. The OR gates allow either the normal shifting operation or the parallel-data entry operation, depending on which the AND gates are enabled by the level on the shift/$\overline{\text{load}}$ input.

It is also known as parallel to serial converter.