10.5 RANDOM ACCESS MEMORY (RAM)

A Random Access Memory (RAM) is a volatile chip memory in which both read and write operations can be performed. Any random memory location can be accessed for information transfer to or from the memory. It is also called *Read-Write Memory* (RWM).

A block diagram of a read-write memory is shown in Fig.10.20(a). It has n address input lines to access 2^n memory locations and m data lines to read/write data from/to memory. The n-bit address is placed in the *Memory Address Register* (MAR) to select one of the 2^n memory locations. Read and Write are control signals that are used to enable memory for read and write operations respectively. When a read is asserted, the data from the memory location, selected by the n-bit address, is placed in Memory Buffer Register (MBR) which is a m-bit register. To perform write operation, the data to be written into a particular memory location is placed in the MBR, and then the write line is asserted. When the write line is asserted, the data in the MBR is written into the memory location, selected by the n-bit address.

Thus, any computer communicates with the memory by means of the memory address register, the memory buffer register and the READ and WRITE inputs. Computers invariably use RAMs for their high-speed main memory and then use backup or slower-speed memories to hold auxiliary data.

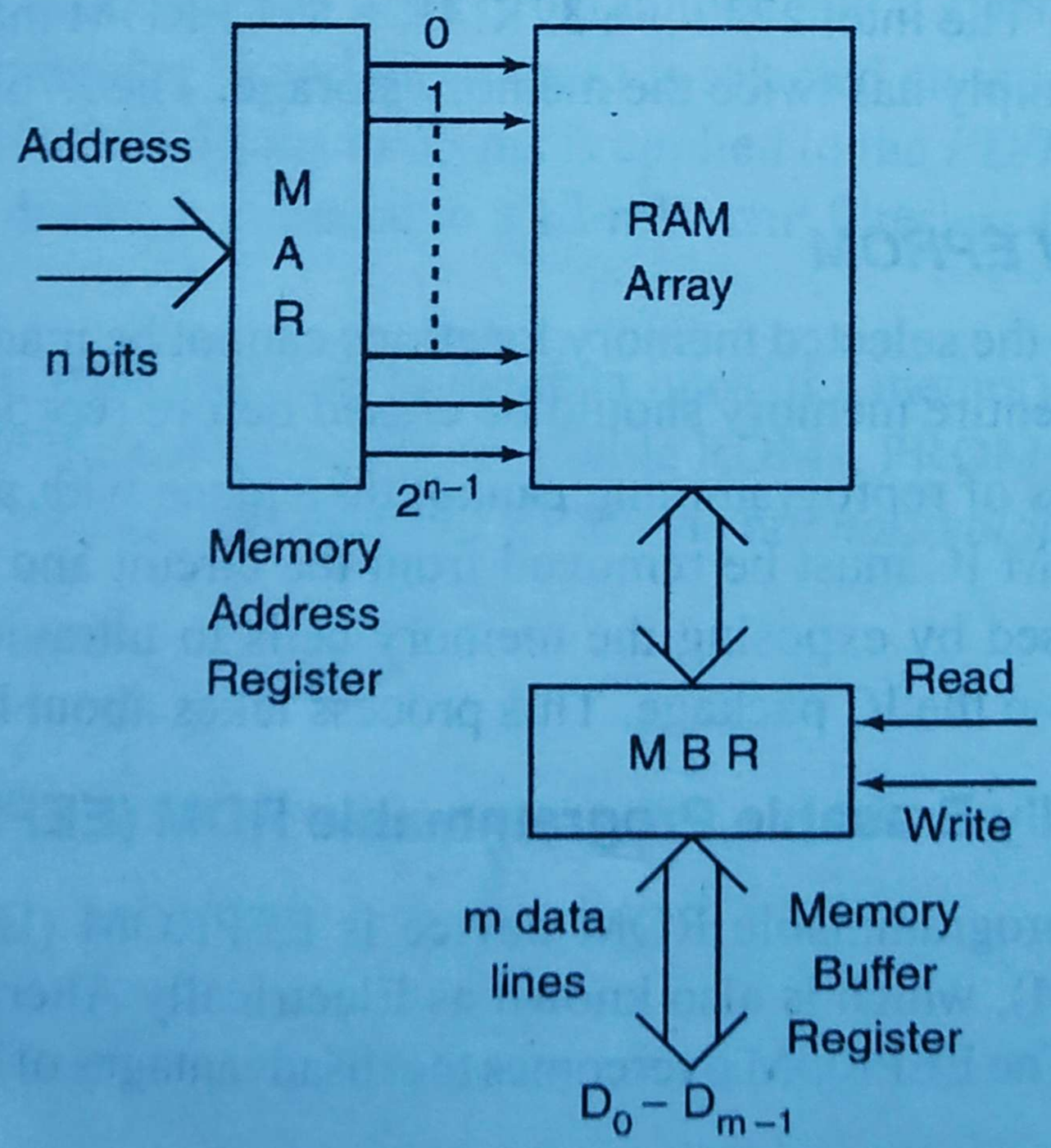

Fig. 10.20(a) *The RAM family*

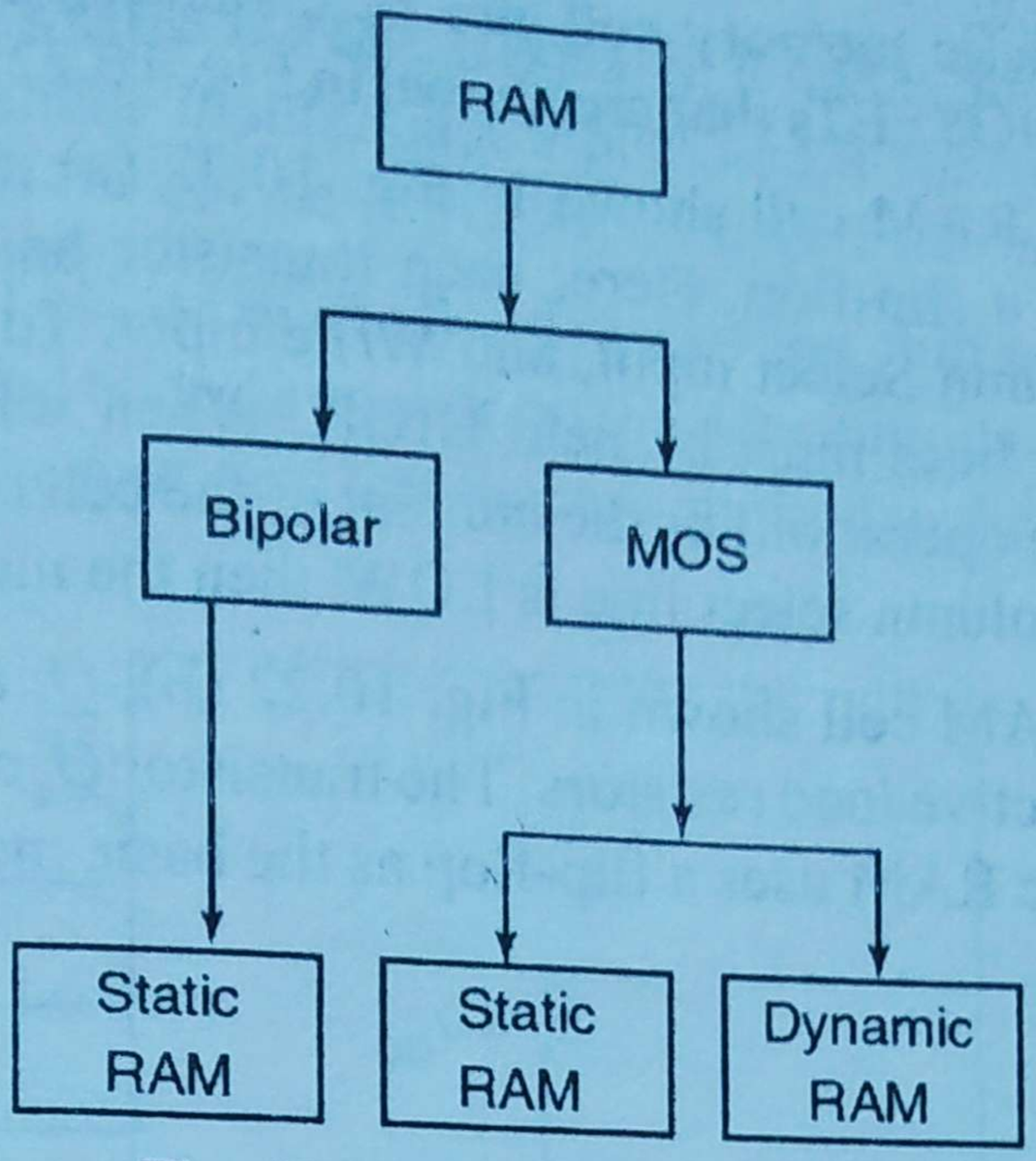

Fig. 10.20(b) The RAM family

10.5.1 Types of RAM

Semiconductor RAMs may be static or dynamic. The static RAM employs bipolar or MOS flip-flops, and the dynamic RAM uses MOSFETs and capacitors that store data. In either case, RAMs are volatile because the stored data will be lost once the d.c. power applied to the flip-flops is removed.

Semiconductor RAMs are available with large storage capacities and have replaced magnetic core memories in most of the computer circuits. The different categories of RAMs are shown in Fig. 10.20(b).

10.5.2 Static RAM

A static RAM essentially contains an array of flip-flops, one for each stored bit. Data written into a flip-flop remains stored as long as a d.c. power is maintained. The memory capacity of a static RAM varies from 64 bits to 1 Mega bit.

Static RAM cell The logic diagram of a static RAM cell is shown in Fig. 10.21. The cell (or a group of cells) is selected by HIGH values on the ROW and COLUMN lines. The input data bit (1 or 0) is written into the cell by setting the flip-flop for a 1 and resetting the flip-flop for a 0 when the READ/$\overline{\text{WRITE}}$ line is LOW (i.e. write). When the READ/$\overline{\text{WRITE}}$ line is HIGH, the flip-flop is unaffected. It means that the stored bit (data) is gated to the *data out* line.

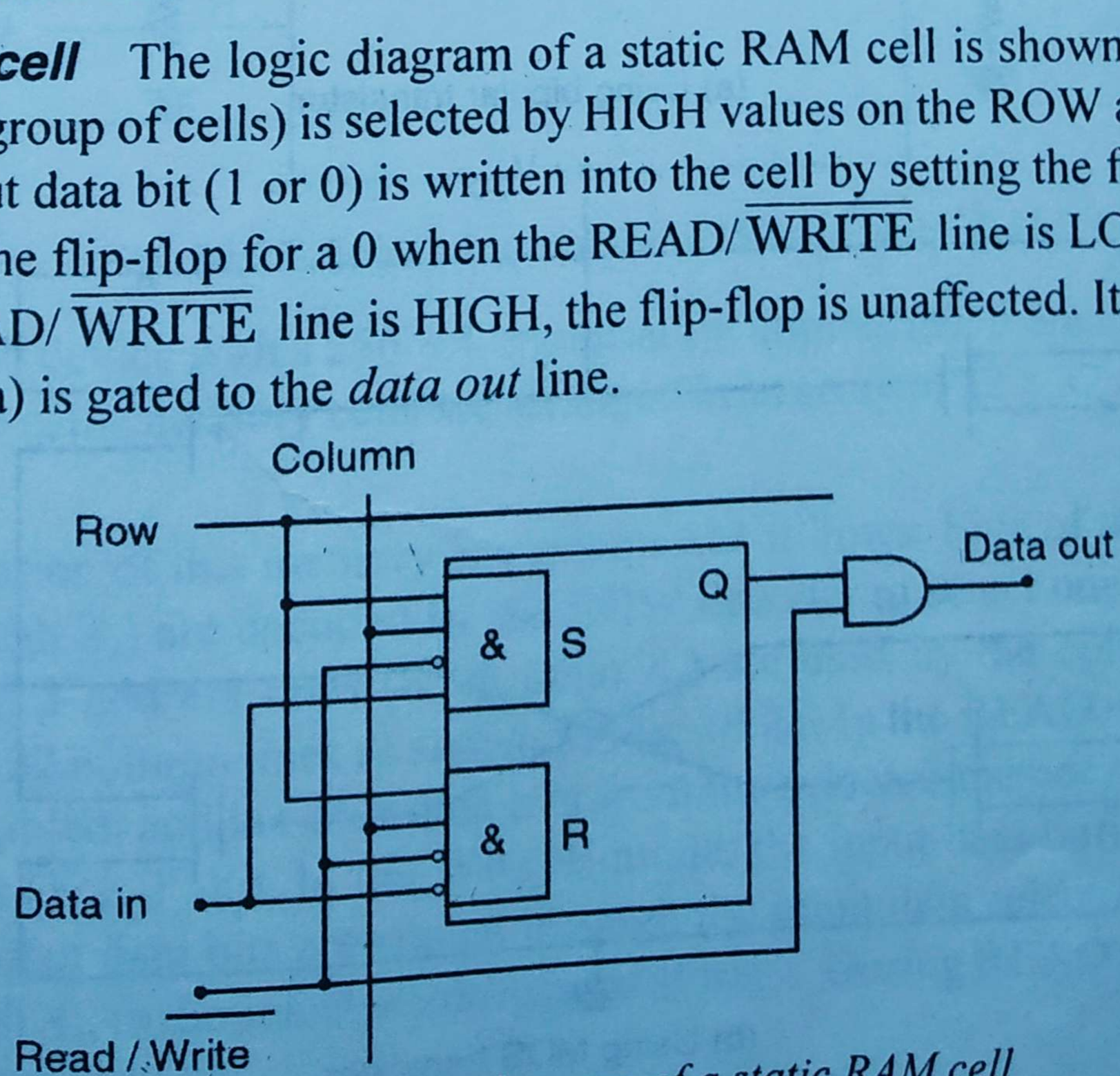

Fig. 10.21 Logic diagram of a static RAM cell

The flip-flop in static memory cell can be constructed using Bipolar Junction Transistor (BJT) and MOSFETs that are shown in Fig. 10.22 (a) and (b) respectively.

In a bipolar static RAM cell shown in Fig. 10.22 (a), two BJTs Q_1 and Q_2 are cross-coupled to form a flip-flop. Here, each transistor has three emitters, namely Row Select input, Column Select input, and Write input. To select the cell, both the row and column select lines must be held HIGH. When selected, a data bit can be stored in the cell (Write operation) or the content of the cell can be read (Read operation). If either row or column select line is LOW, then the memory cell is disabled.

In a MOS static RAM cell shown in Fig. 10.22 (b), Q_1 and Q_2 act like switches while Q_3 and Q_4 act as active load resistors. The transistor Q_1 conducts and Q_2 is cut off or vice versa. As a static RAM uses a flip-flop as the basic memory cell, it consists of thousands of flip-flops.

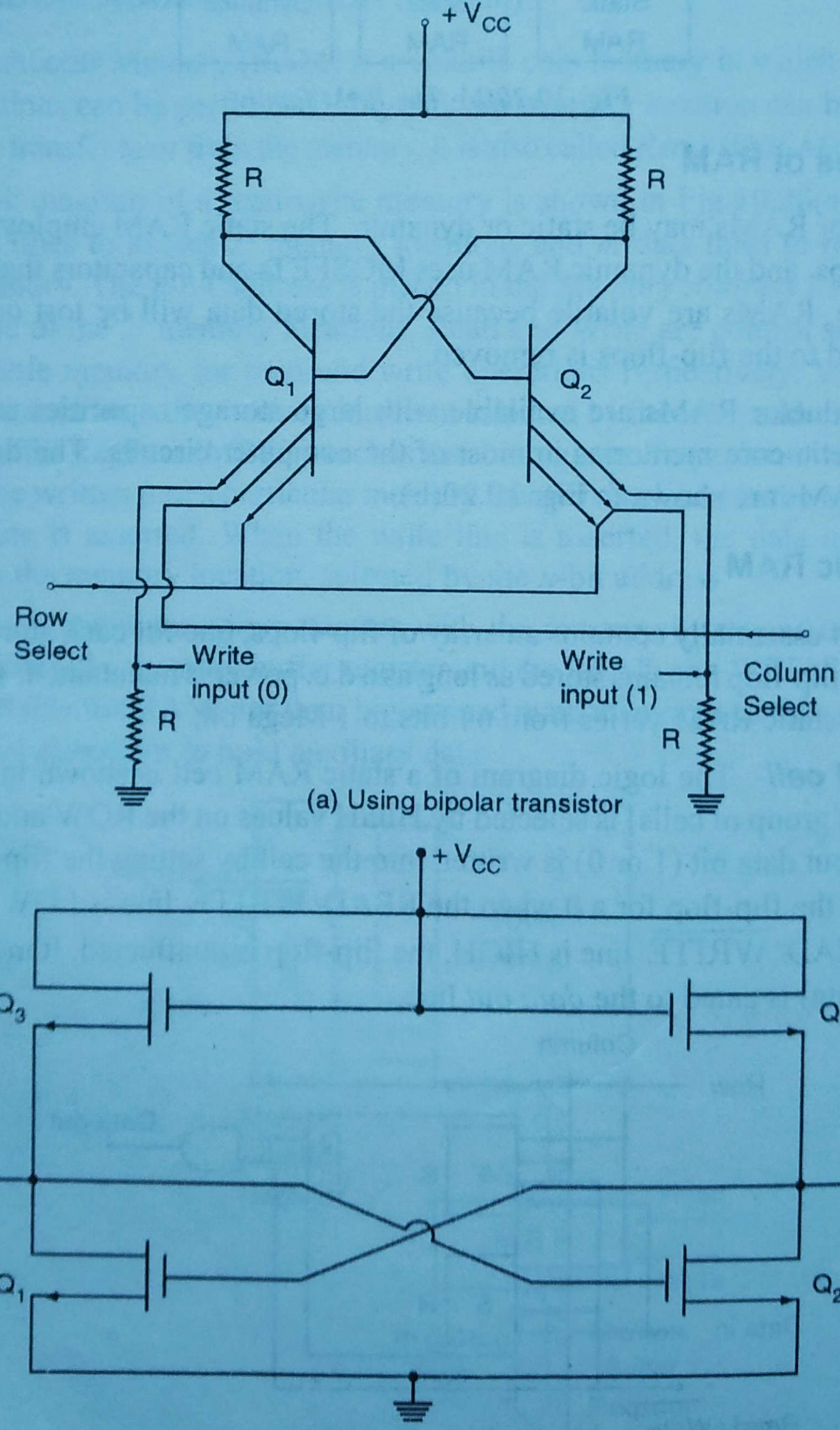

Fig. 10.22 Static RAM cell

Basic structure of a static RAM Basically, RAM is addressed in the same way as ROM. RAM has address inputs, data inputs and a READ/WRITE control. The logic diagram for a 1024-bit device with 256 × 4 organisation is shown in Fig. 10.23.

When READ/$\overline{\text{WRITE}}$ is HIGH (Read mode) and chip select ($\overline{CS}$) is LOW, four data bits from the selected address appear on the data outputs. When READ/$\overline{\text{WRITE}}$ is LOW (write mode), the four data bits that are applied to the data inputs are stored at the selected address.

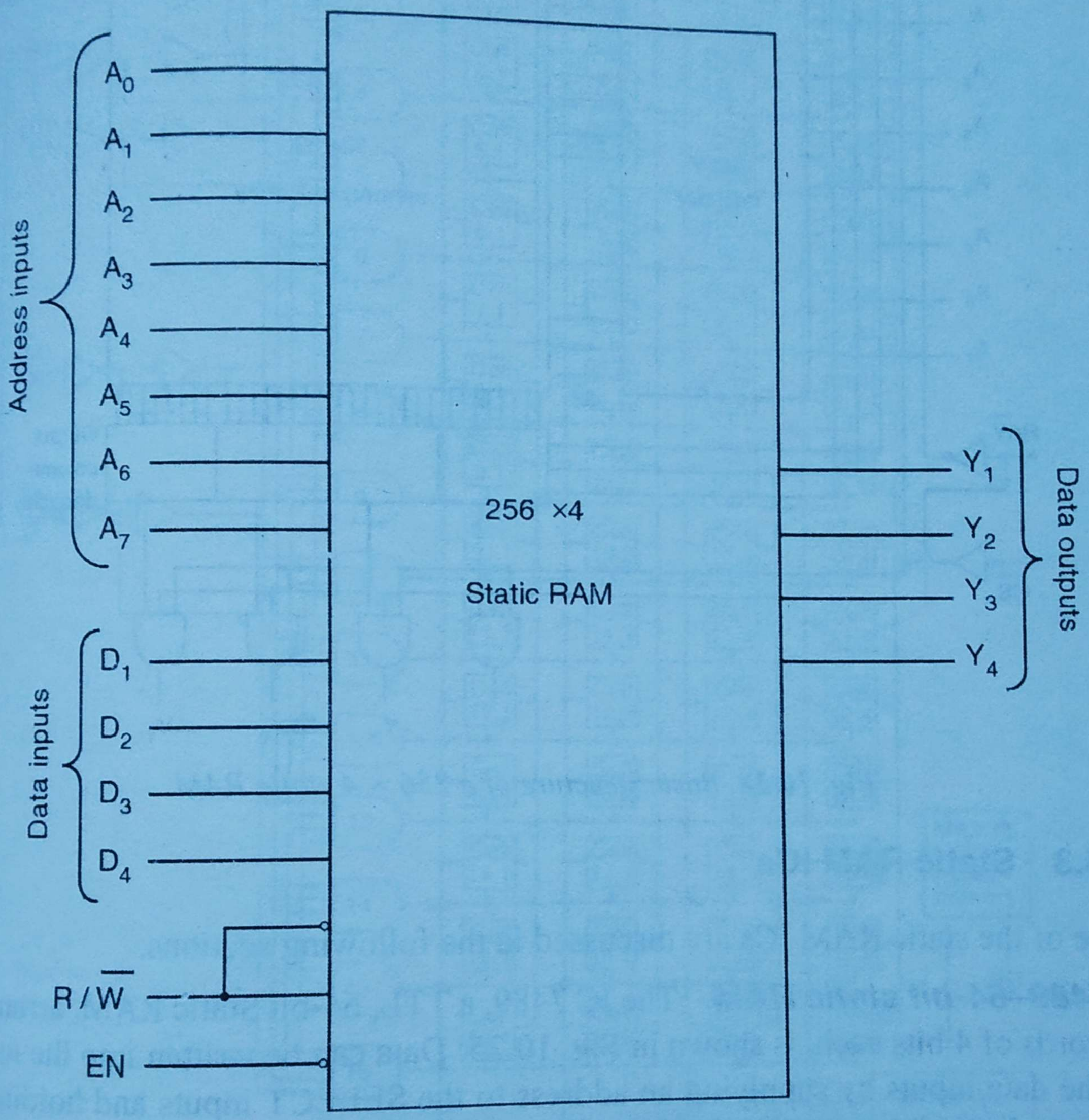

Fig. 10.23 *Logic diagram for a 256 × 4 static RAM*

A 1024-bit device with a 256 × 4 organisation implies that there are 256 rows and 4 columns. Here, the memory cells are arranged in an array of 32 × 32 matrix as shown in Fig. 10.24.

The operation of this memory is explained as follows: Five of the eight address lines (A_0 through A_4) are decoded by the ROW decoder to select one of the 32 rows. The remaining 3 address lines (A_5 through A_7) are used by the column decoder to select 4 of the 32 column lines as shown in Fig. 10.24. In the READ mode, the output buffers are enabled, and the four data bits from the selected memory location appear on the outputs ($Y_4\ Y_3\ Y_2\ Y_1$). In the WRITE mode, the input data buffers are enabled, and the four input data bits are routed through the input data selector by the address bits, A_5 through A_7, to the selected address for storage. During READ and WRITE, the chip select must be LOW.

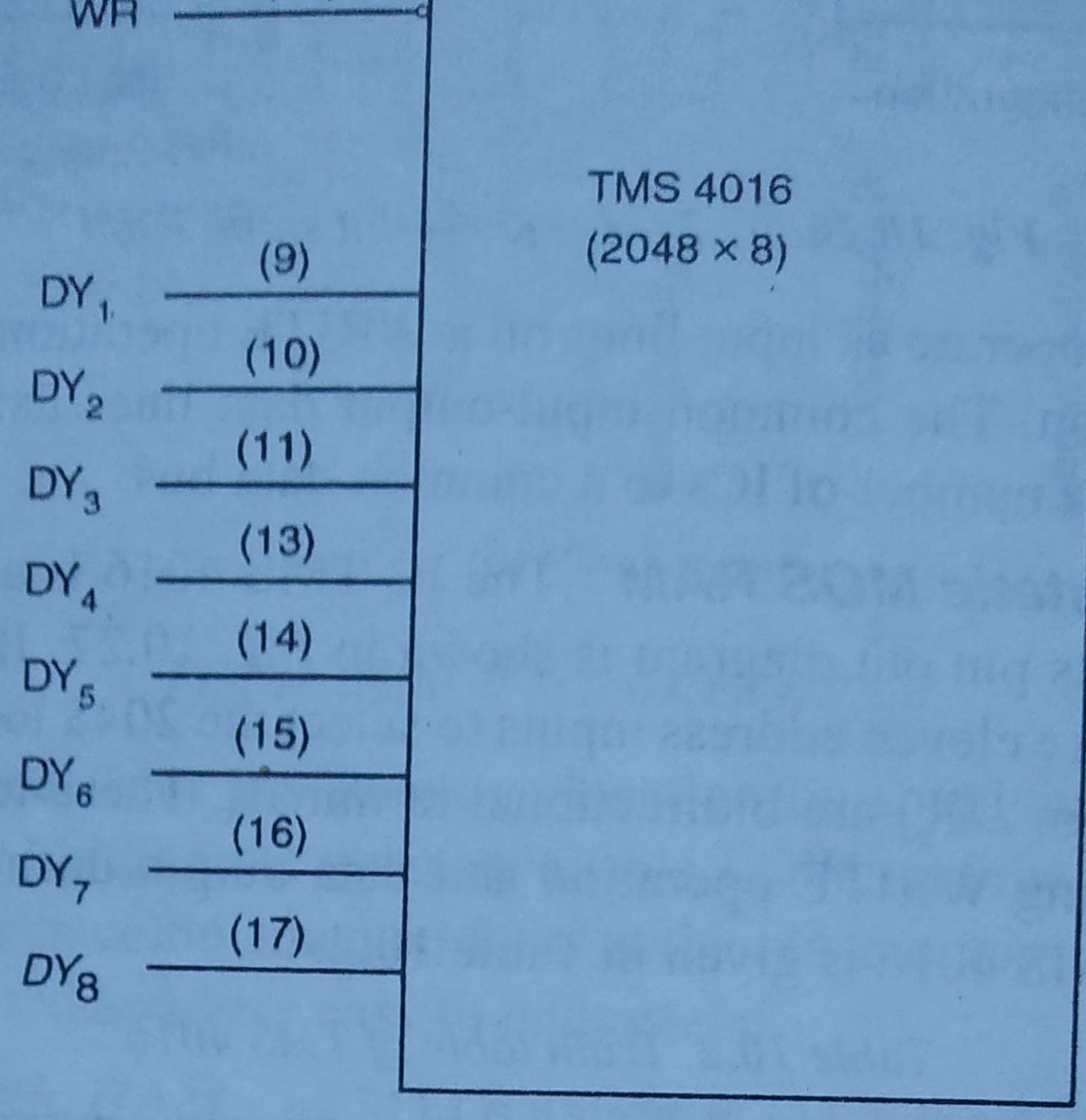

Fig. 10.27 TMS 4016—2 KB MOS static RAM

10.5.4 Dynamic RAM (DRAM)

The Dynamic Random Access Memory (DRAM) is the lowest cost, highest density random access memory available. Nowadays, computers use DRAM for main memory storage with the memory sizes ranging from 16 to 256 Mega bytes.

The DRAM stores its binary information in the form of electric charges on capacitors. Data are stored as charge on every capacitor, which must be *recharged* or *refreshed* thousands of times every second in order to retain the stored charge. These memory devices make use of an integrated MOS capacitor as basic memory cell instead of a flip-flop. The advantage of this cell is that it allows very large memory

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arrays to be constructed on a chip at a lower cost per bit than in static memories. The disadvantage is that the MOS capacitor cannot hold the stored charge over an extended period of time and it has to be refreshed every few milliseconds. This requires more circuitry and complicates the design problem. Static RAMs are simpler than dynamic RAMs.

A typical dynamic RAM cell consisting of a single MOSFET and a capacitor is shown in Fig. 10.28. A dynamic RAM consists of an array of such memory cells. In this type of cell, the transistor acts as a switch. The memory cell also requires MOSFETs for READ and WRITE gating to operate the cell. Data input is connected for storage by a WRITE control signal.

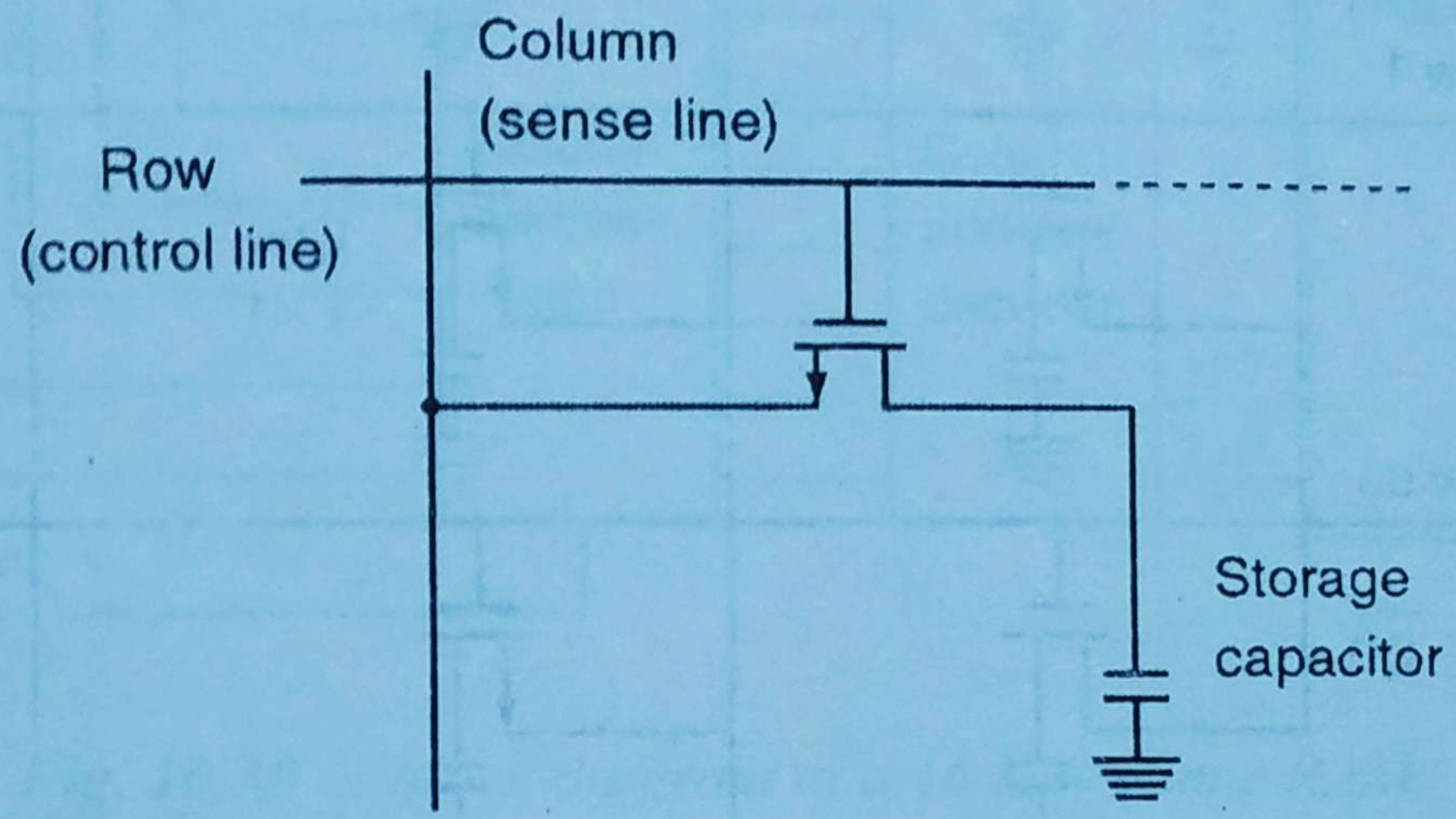

Fig. 10.28 *A dynamic MOS RAM cell*

The Dynamic RAM offers reduced power consumption and large storage capacity in a single memory chip. With the availability of such high packing density memory ICs, the capacity of memory will continue to grow.

Dynamic memory organisation The organisation of a dynamic memory allows many cells to be accessed by a minimum amount of circuitry. Each memory cell is gated onto a data input/output line when a ROW and a COLUMN select MOSFETs are driven ON as shown in Fig. 10.29. For example, to select the DRAM cell marked 1–1, a 1 (HIGH) has to be applied at ROW 1 and COLUMN 1 select inputs. A HIGH at ROW 1 input selects all 128 transistors connected to the ROW 1 select line while the HIGH at the COLUMN 1 input selects one of the 128 possible COLUMNs, thereby the cell marked 1–1 being read onto the I/O data line. A sense amplifier for each column is necessary to convert from the low voltage and low energy to a sufficient level voltage on the I/O data line. The circuitry interposed between a bit-storage capacitor and external data line is called a *sense amplifier*. A matrix of 64 × 128 accounts for 8192 individual memory cells, and only one cell is connected onto the data line at any time.

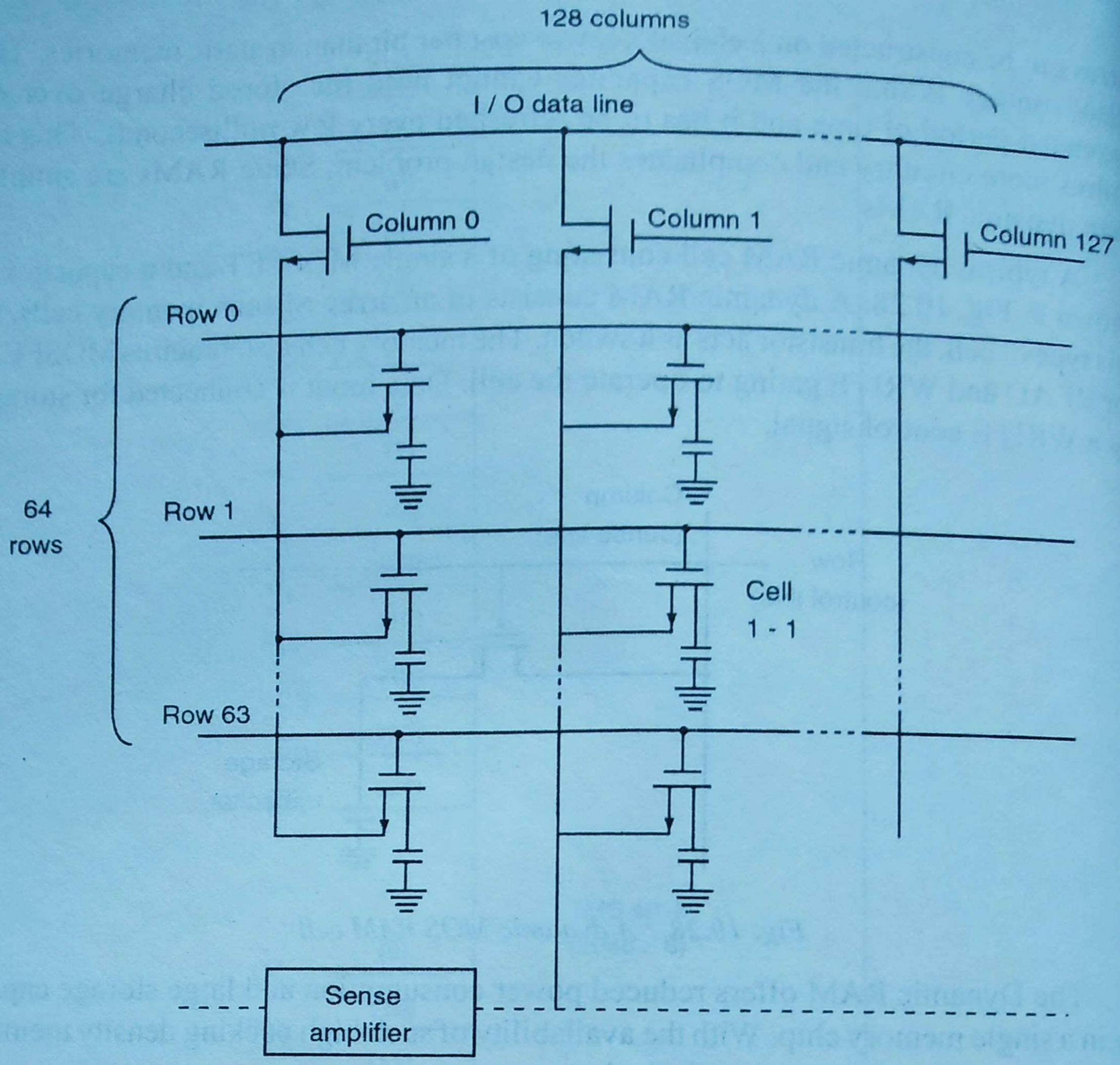

Fig. 10.29 ROW and COLUMN selection of a DRAM cell

The column and row decoders together selects a single capacitor and provide access to that 1-bit storage site for reading and writing. All the capacitors in an entire row can be refreshed simultaneously. There is a provision on the chip for activating all the sense amplifiers simultaneously and closing simultaneously all the appropriate switches in the bit lines. Such simultaneous activation will refresh all the capacitors in the ROW selected by the ROW decoder.

Basic structure of a dynamic RAM A Dynamic RAM usually employs a technique called *address multiplexing* to reduce the number of address lines and thus the number of input/output pins on the IC package.

A block diagram of a 16 K bit (16,384 bits) dynamic RAM that has been simplified to illustrate address multiplexing is shown in Fig. 10.30. Since $2^{14} = 16{,}384$, the fourteen-bit address is applied (seven bits at a time) to the address inputs. First of all, the seven-bit ROW address has to be applied and the $\overline{RAS}$ (row address strobe) latches the seven bits into the ROW *address latch*. Next, the seven-bit COLUMN address is applied to the address inputs, and the $\overline{CAS}$ (column address strobe) latches the remaining seven bits into the COLUMN *address latch*. Then, the seven-bit ROW address and the seven-bit COLUMN address are decoded to select the appropriate memory cell in the 128 × 128 dynamic memory array for a READ or WRITE operation. The timing diagram of the address multiplexing operation is shown in Fig. 10.31.

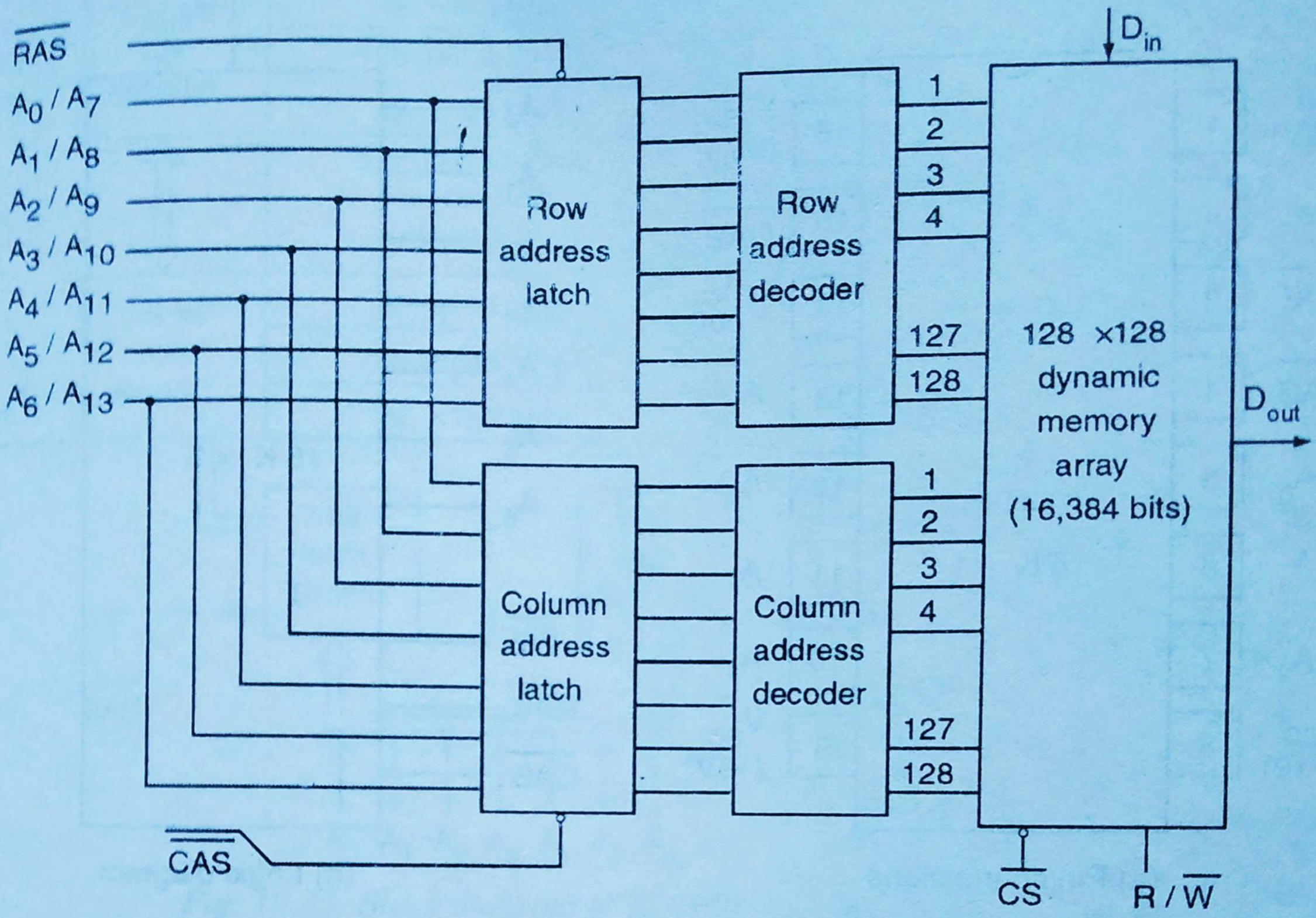

Fig. 10.30 *A block diagram of a 16 K dynamic RAM*

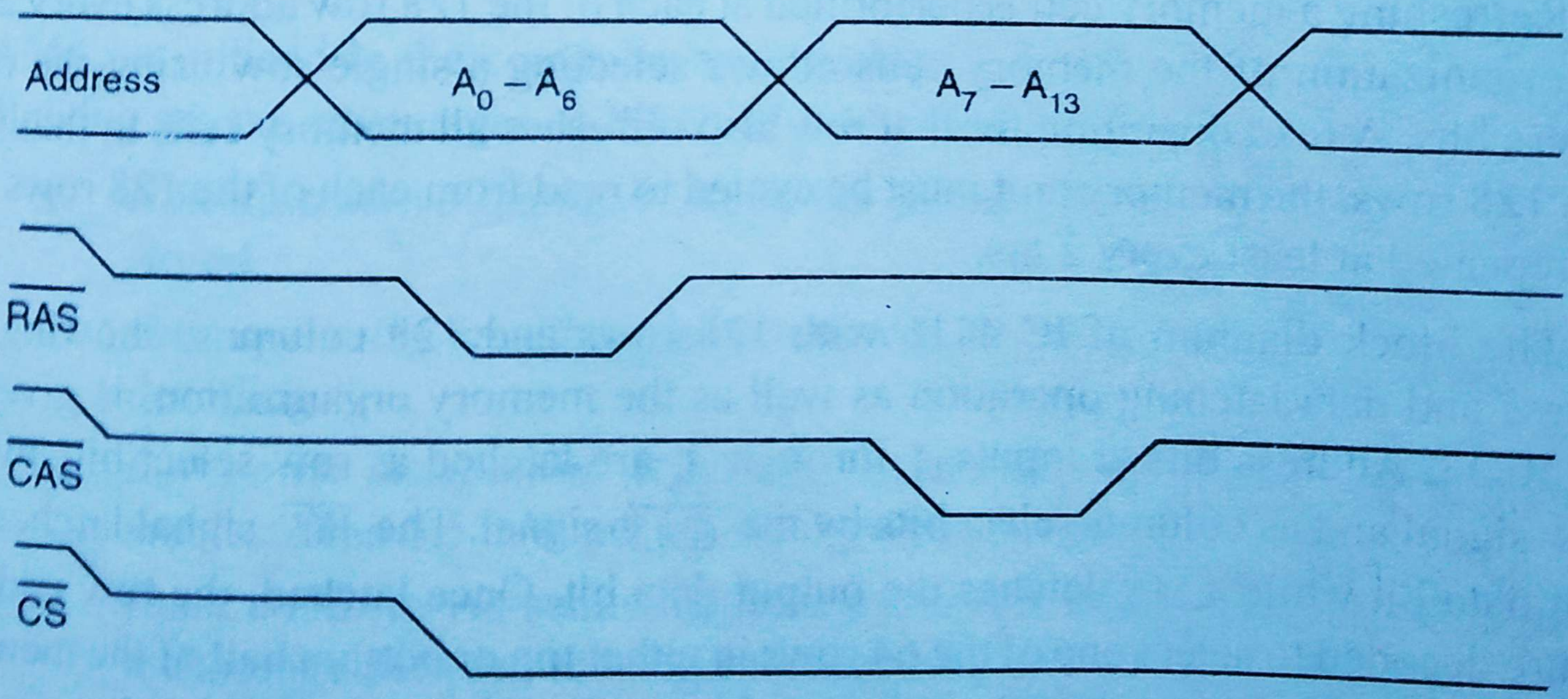

Fig. 10.31 *Timing diagrams for address multiplexing in DRAM*

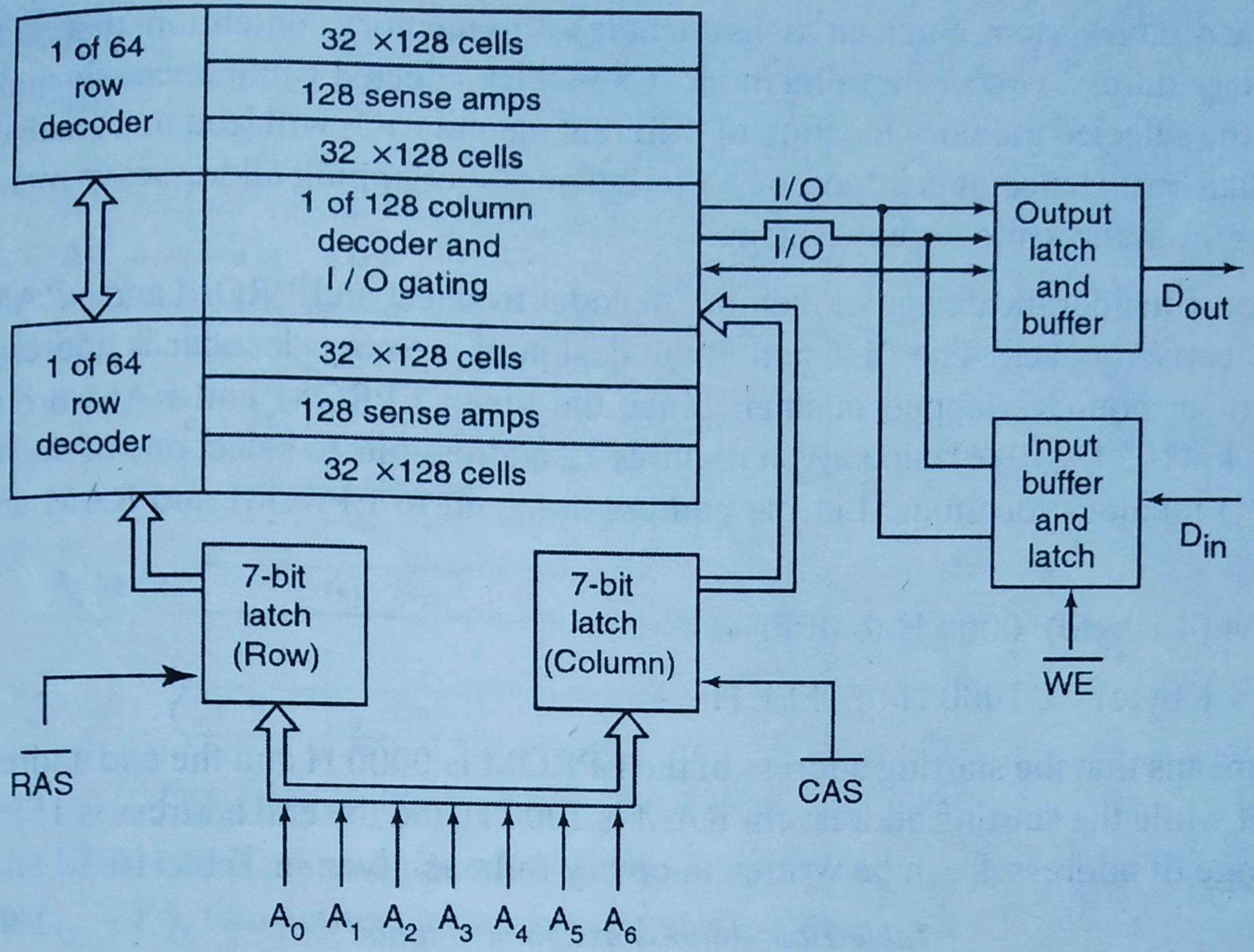

Fig. 10.33 Block diagram of IC 4116–16K × 1 dynamic memory

10.5.6 Advantages of RAM

RAMs are utilized in the computer as scratch-pad, buffer and main memories. The following are the advantages of MSI/LSI RAMs over magnetic devices:

1. *Non-destructive read out*: Read out of a RAM does not affect the content stored.
2. *Fast operating speed*: Access time can be as low as 150 ns, with on-chip decoding.
3. *Low power dissipation*: It is typically less than 1mW per bit for static RAM and less than 0.5 mW per bit for dynamic RAM.
4. *Compatibility*: As semiconductor memories enjoy common interface and technology between sensing and decoding circuitry and the storage element itself, they are self-compatible.
5. *Economy*: MOS memories are more economical than magnetic core for small and medium-sized systems.