10.4.9 Programmable ROM (PROM)

In order to provide some flexibility in the possible applications of ROM, programmable ROMs (PROMs) have been introduced. The PROM can be programmed electrically by the user but cannot be reprogrammed. In a PROM chip, the manufacturer includes a connection at every intersection of the grid of address and data lines. PROMs are widely used in the control of electrical equipment such as washing machines and electric ovens.

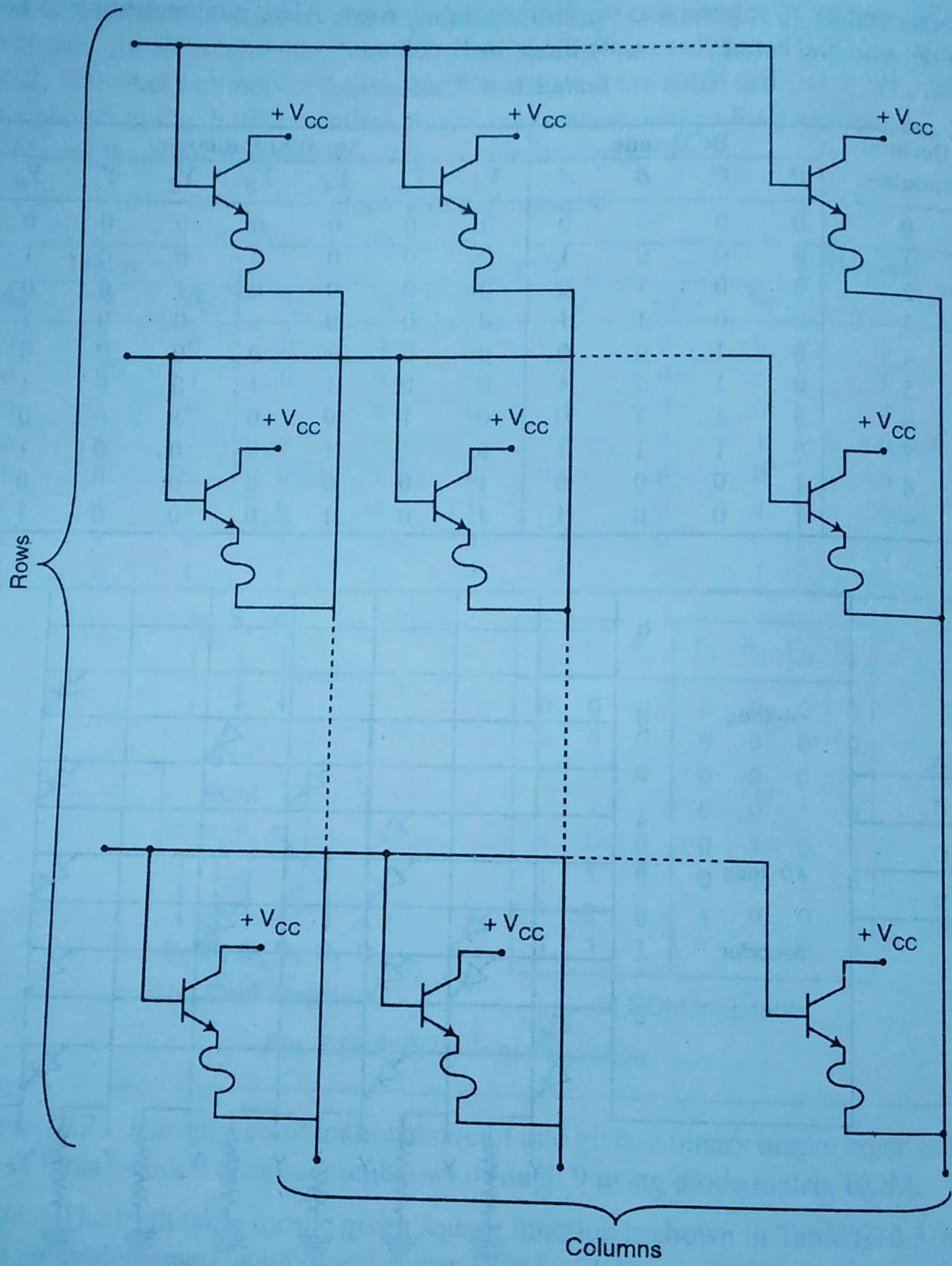


Fig. 10.13 *Bipolar PROM array with fusible links*

PROMs are available in both bipolar and MOS technologies. PROMs have 4-bit or 8-bit output word formats with capacities ranging in excess of 2,50,000 bits. A PROM is manufactured as a generalised integrated circuit with all the matrix intersections linked by *fusible* diodes or transistors. In series with each connection, the manufacturer includes a fusible link which can be melted, and thereby opened, by passing a large current through it. A memory link is fused open or left intact to represent a binary number 0 or 1. The user can selectively *burnout* some of the fuses by passing enough current through them and can thereby program the PROM according to the required truth table. Once a PROM is programmed, it cannot be changed, and therefore it has to be done carefully and correctly in the first time itself. Hence, the fusing process is irreversible.

Fuse technology used in PROM A bipolar PROM array with *fusible links* is illustrated in Fig. 10.13. In PROM, the fuse links are placed between the emitter of each cell's transistor and its column line. The cell type is called a *fuse cell.*

The following are the three basic fuse technologies used in PROMs:

(i) metal links

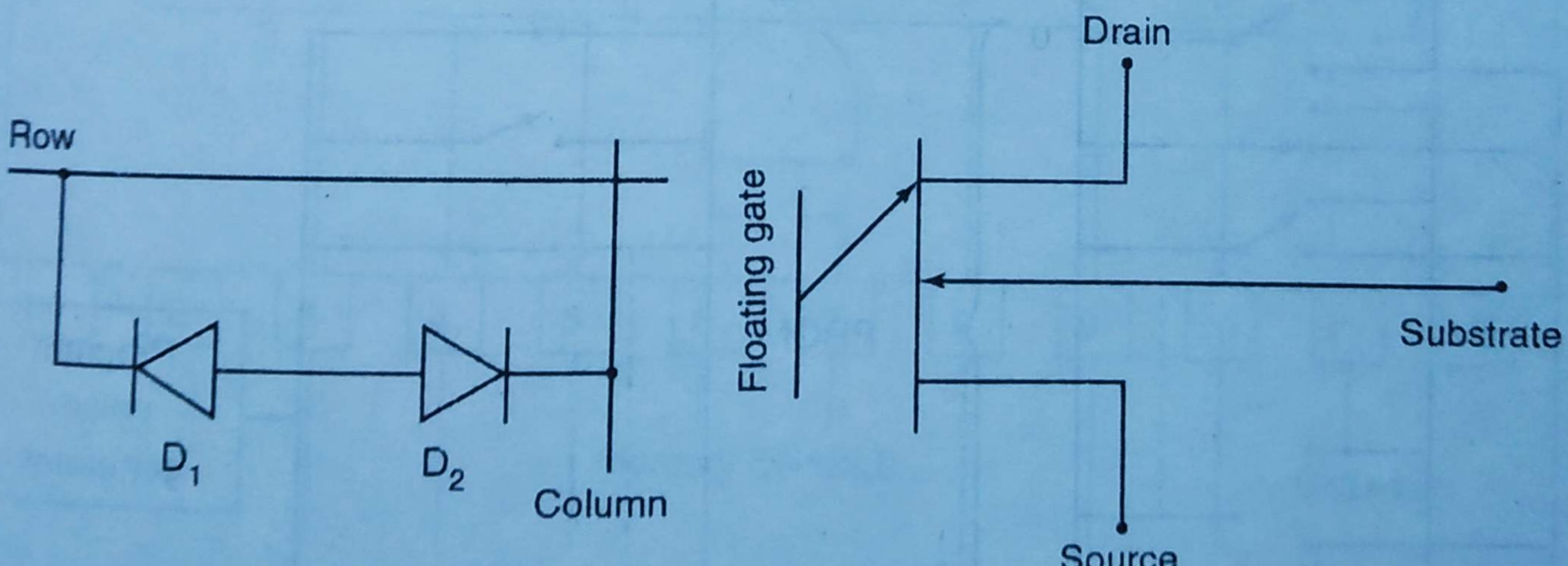
(ii) silicon links

(iii) *p-n* junctions.

Metal links are made of a Nichrome material. Each bit in the memory array is represented by a separate link. The metal link is either "blown" open or left intact during programming. This is done basically by addressing a given fuse cell and then forcing sufficient amount of current through the link to make it open.

Silicon links are formed by narrow notched strips of polycrystalline silicon. Programming of silicon links requires melting of the links by passing enough amount of current (20–30 mA) through them. The current causes a high temperature (1400°C) at the fuse location, and the silicon gets oxidized and forms an insulation around the new open link.

p-n junctions This technology, also referred to as shorted junction or avalanche-induced migration, consists of two *p-n* junctions arranged back to back as shown in Fig.10.14(a). During programming, the *p-n* junction of diode D_1 is avalanche reverse-biased. The sudden heavy flow of electrons in the reverse direction and heat cause aluminium ions to migrate and short the junction of the emitter-base. The current is of the order of 200–300 mA. The other *p-n* junction is forward-biased, and this diode can be used to represent a data bit.



(a) A shorted junction cell (b) Symbol of FAMOS ROM

Fig. 10.14

The above fuse technologies are irreversible. These technologies do not work with MOS memory devices where high current levels required for the fusing process are incompatible with MOS impedance levels. The following are the MOS technologies used for the fabrication of programmable memories:

(i) Floating Gate Avalanche Injection MOS (FAMOS) and

(ii) MAOS.

FAMOS ROM This is the storage device used in silicon gate MOSFET with no electrical connection to the gate, i.e. the gate is electrically floating in an insulating layer of silicon dioxide. The symbol of FAMOS ROM is shown in Fig. 10.14(b).

MAOS PROM A MOS memory cell using alumina ($Al_2 O_3$) as gate dielectric is called a MAOS memory element. This gate dielectric is used for charge storage and provide a reprogramming feature. The MAOS element is programmed by the application of a positive or negative gate voltage pulse above a threshold level, as per the specifications of that PROM.

10.4.10 PROM Programming

A PROM is programmed by plugging it into a special device called *PROM Programmer*. The programming is accomplished by using a simplified set up shown in Fig. 10.15. An address is selected by the switch settings on the address lines (0 through *m*) and then a pulse is applied to those output lines corresponding to bit locations where 1s are to be stored. The PROM actually starts out with all 0s. These current pulses blow the fuse links, thus creating the desired bit pattern. The next address is then selected and the process is repeated. This sequence is done automatically by the PROM programmer.

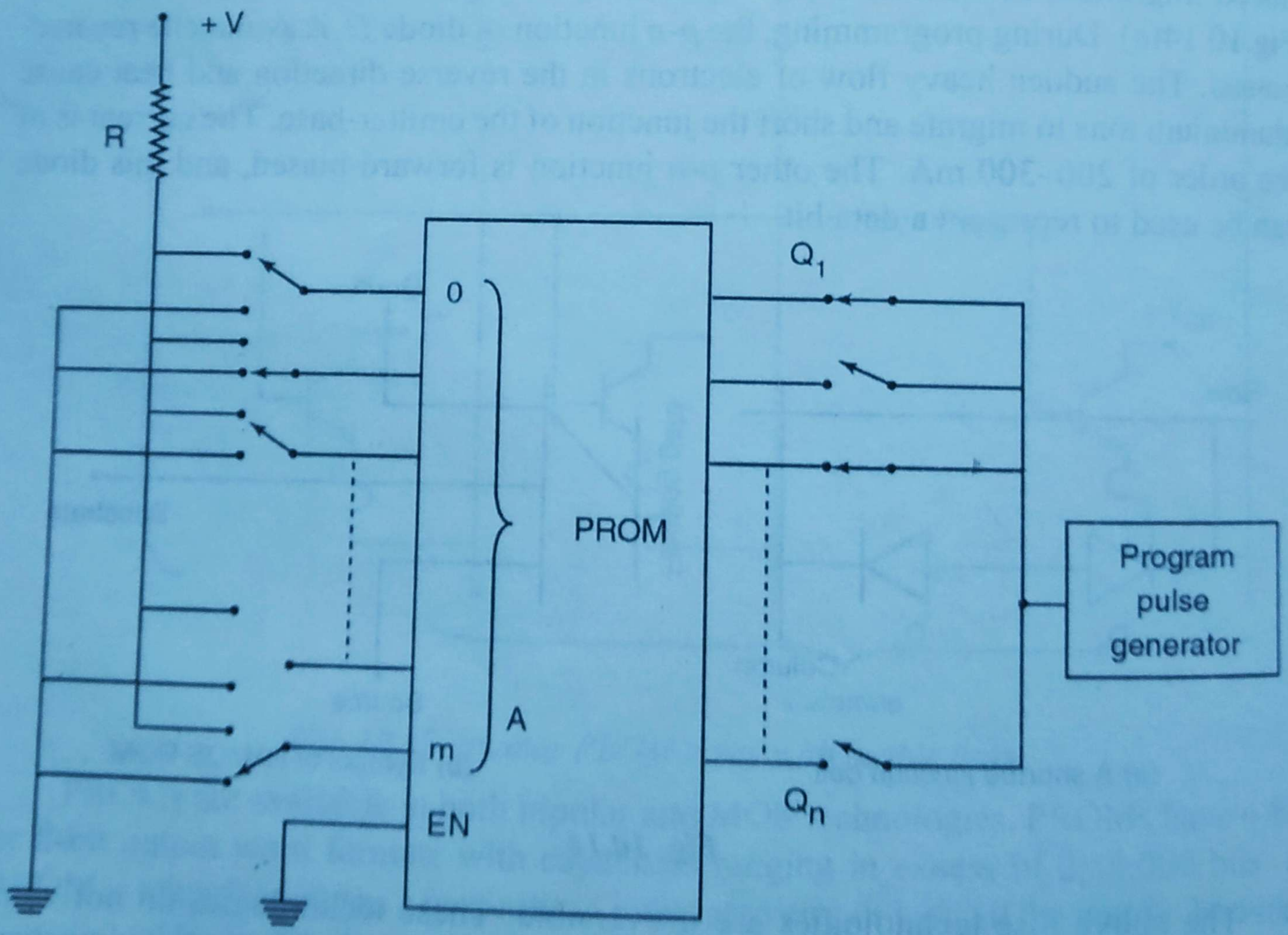


Fig. 10.15 Simplified PROM programming set up

IC 74186–512-bit PROM The IC 74186 is a TTL LSI 512-bit PROM. It is organised as 64 words of 8 bits each. The logic diagram of this IC PROM is shown in Fig. 10.16(a). The 6 bits of address (*A*, *B*, *C*, *D*, *E* and *F*) are decoded to uniquely select one of the 64, 8-bit words in a linear addressing scheme.

The chip is initially stored with full of 0s, i.e. the contents of any 8-bit word is 0000 0000. We know that the programming is done by applying current pulse to each output terminal where a logic 1 appears. The IC 74186 PROM is programmed using the following procedure as shown in Fig. 10.16(b).

1. First of all, apply the correct address (*ABCDEF*) for the word to be programmed. For instance, if the desired contents of word 29 is 1001 1011, the address would be 0001 1101. A 0 is a closed switch and a 1 is an open switch.
2. Apply a current pulse to each bit to store a 1.
3. Repeat the above steps for all words to be stored in the memory.

Specific information such as current pulse limits, voltage levels and so on for chip (IC) programming must be taken from the manufacturer's specification sheets.

Once the field programming is done, it cannot be altered.

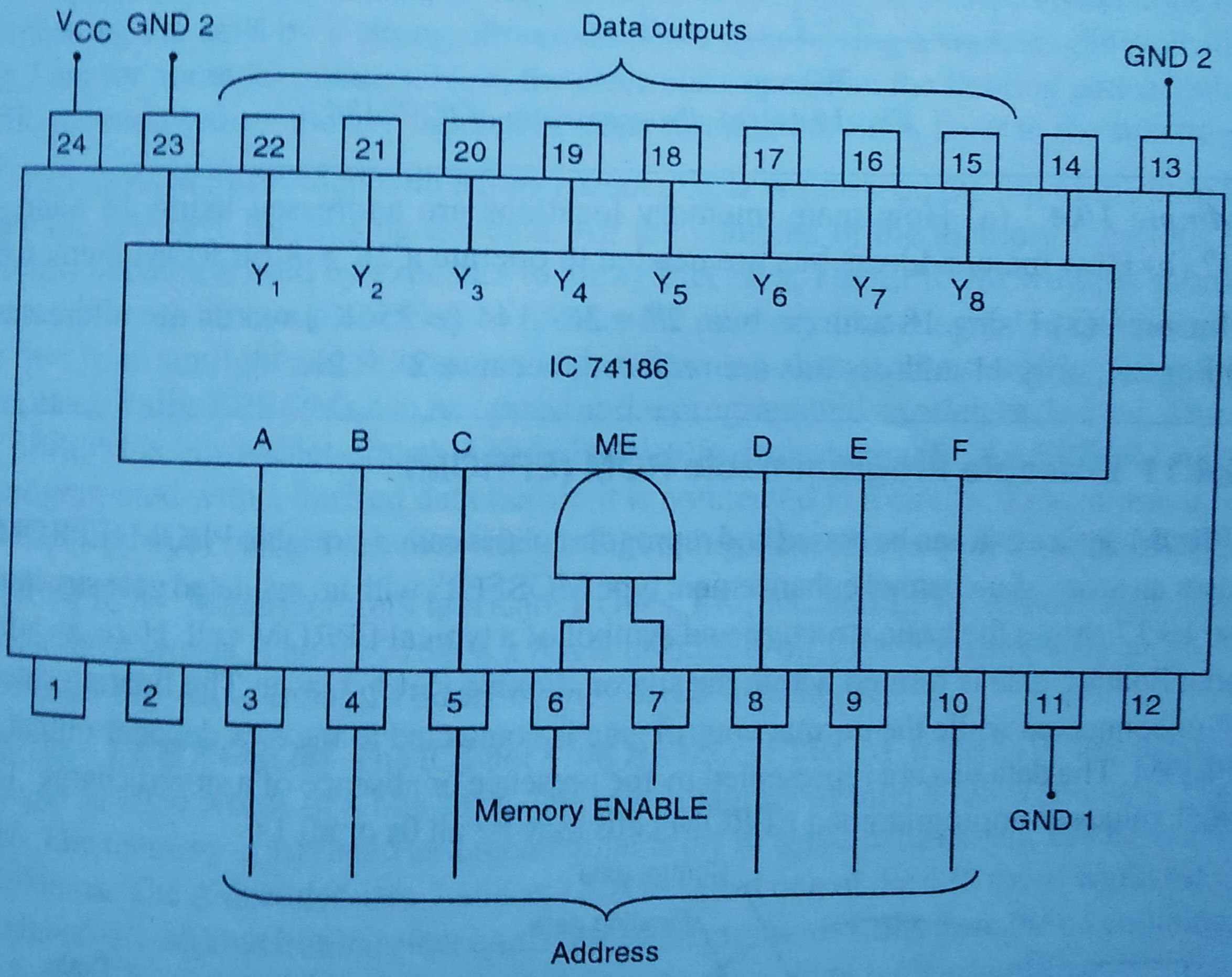


Fig. 10.16 (a) *Logic and pinout diagrams*

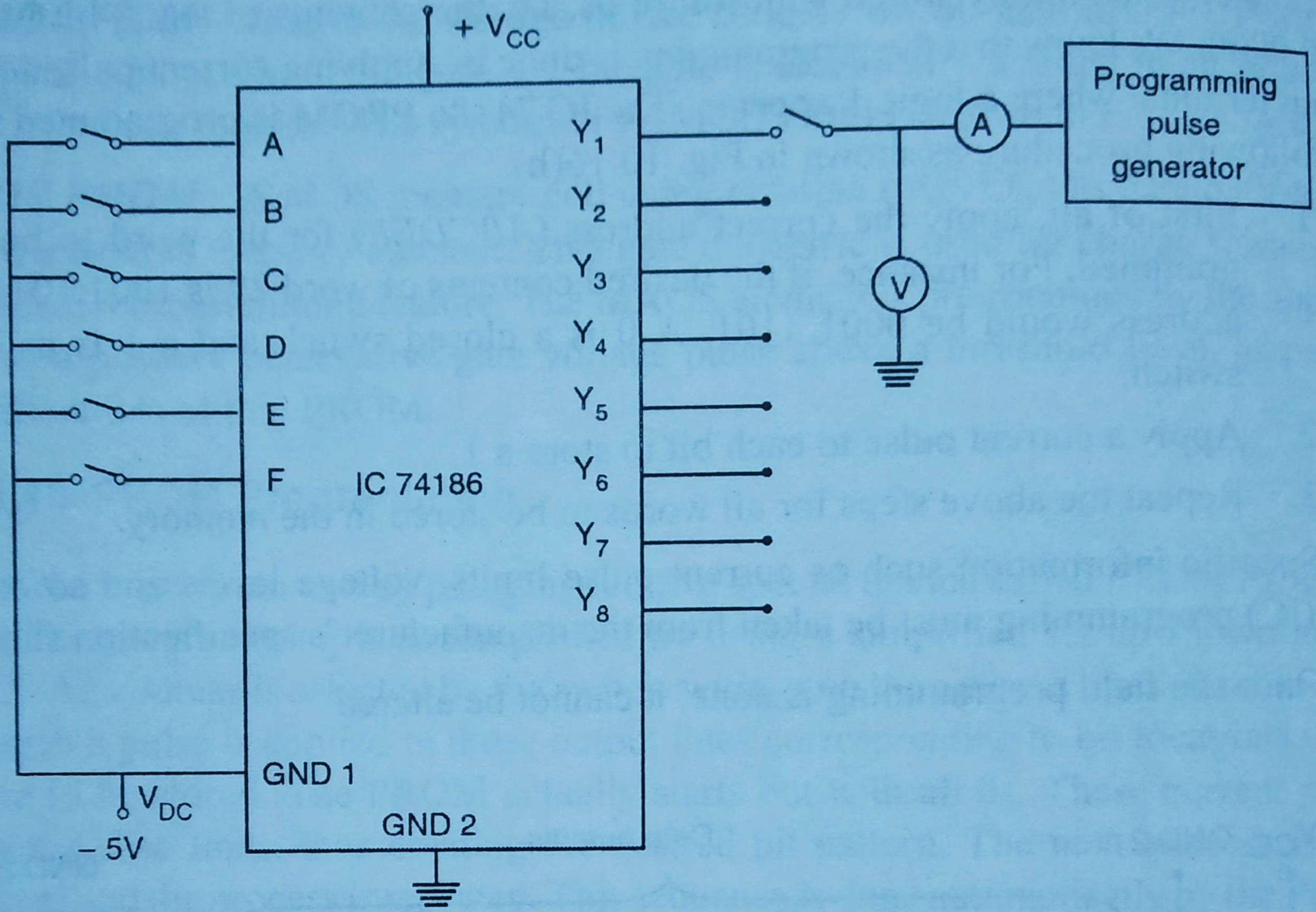


Fig. 10.16 (b) *Programming of IC 74186*

10.4.11 Erasable Programmable ROM (EPROM)

A PROM device that can be erased and reprogrammed is called Erasable PROM (EPROM). It uses an array of *n*-channel enhancement type MOSFETs with an insulated gate structure. Fig. 10.17 shows the basic structure and symbol of a typical EPROM cell. Here, an additional floating gate is formed within the silicon dioxide (SiO_2) layer. The floating gate is left unconnected while the normal control gate is connected to the row decoder output of EPROM. The data bits are represented by the presence or absence of a stored charge. The initial values of unprogrammed EPROM cells may be all 0s or all 1s.

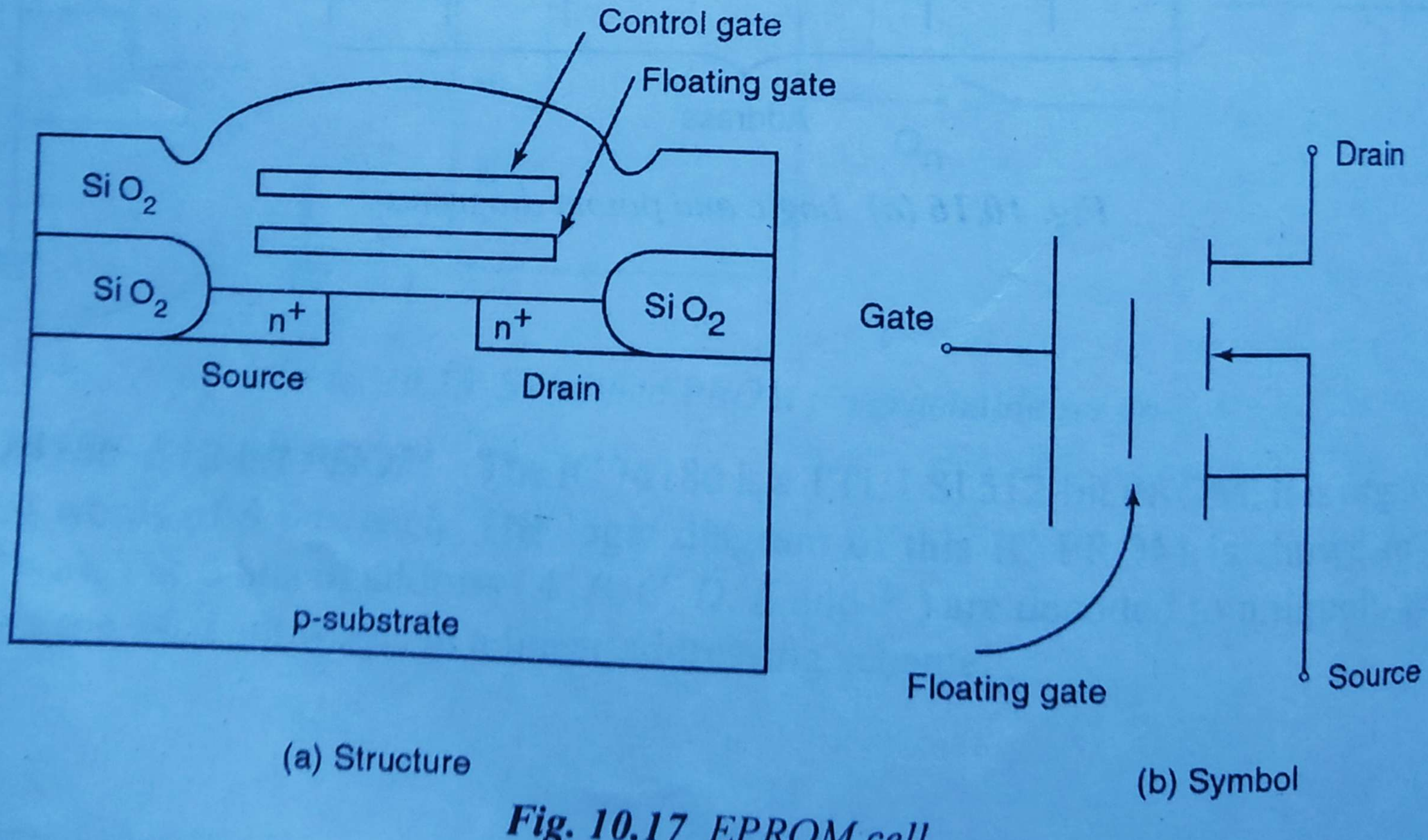


Fig. 10.17 EPROM cell

10.4.12 Programming of EPROM

Consider the programming of an EPROM with 1s as initial values in all the cells. To program or store a 0 in such a cell, the floating gate must be charged. For this, a high voltage of about 16 to 20V is applied between the source and drain, and a voltage of about 25 to 50V is applied to the control gate for a specified amount of time (typically 50ms per address location). Due to the high electric field established by the positive control gate voltage, the high energy electrons penetrate the thin insulating SiO_2 and reach the floating gate. Thus, the charge is stored on the floating gate. Since more negative charge accumulates on the floating gate, the electric field strength is reduced, and thereby further accumulation is inhibited. Programming actually involves selecting the desired cell gate and repeatedly injecting charge onto the floating gate until a sufficient amount of charge is trapped. Since the gate is surrounded by SiO_2, there is no discharge path available. Therefore, the charge remains trapped on the floating gate for an indefinite period of time. Now, the cell is programmed for a logic 0.

To program a different data, all cells in the EPROM must be erased. This is done by illuminating the cells by a strong ultraviolet (UV) light having a wavelength typically 253.7 nm for about 20 minutes. Now, the electrons trapped on the floating gate acquire sufficient energy from the UV light and escape through the SiO_2 layer to the substrate.

EPROMs are provided with a transparent quartz window on the top of the chip to allow the UV rays for erasing the data. All the contents of the memory locations in EPROM become erased by exposure to ultraviolet rays. The EPROM window should be covered with an opaque sticker to protect the memory from unwanted exposure to UV rays from sunlight and fluorescent lamps. The new data can be stored by programming electrically. EPROMs can be erased and reprogrammed as often as desired. Thus, the EPROM is ultraviolet-erasable and electrically programmable. An EPROM must be programmed with a desired data before it is connected in a circuit. Programming is done byte by byte using a set of switches for setting data bits as well as address bits.

EPROM ICs Manufacturers fabricate ROMs, PROMs and EPROMs that can store thousands of words. The IC 2764 is a 8 KB or 65536-bit EPROM organised as 8192 words of 8 bits each. It has 13 address lines and 8 data lines.

IC 8708 – 1 KB EPROM The IC Intel 8708 is a MOS EPROM. It has 8192 bits that are arranged as 1024 words of 8 bits each. The logic diagram of Intel 8708 is shown in Fig. 10.18. The memory is arranged as a rectangular array of 8,192 cells having 128 rows and 64 columns. The *X* decoder uses 7 address bits to select one of the 128 rows, while the *Y* decoder uses 3 address bits to select one of the eight groups of 8 bits from the 64 columns. The 8 data bits are available at the outputs through three-state buffer amplifiers.

Access time The access time is the time taken to read a stored word after applying the address bits. Bipolar memories have faster access time than MOS memories. The Intel 8708 is a MOS EPROM with an access time of 450 ns. The Intel 2716 is also a MOS EPROM with an access time of 450 ns. The 3636 is a bipolar PROM with an access time of 80 ns. The Intel 2732 is a 32K(4K × 8) EPROM that is pin-compatible with the 2716—it simply has twice the memory storage. The 2764 is a 64K (8K × 8) EPROM.

Disadvantages of EPROM

(1) Changes in the selected memory locations cannot be made in the reprogramming. The entire memory should be erased before reprogramming.

(2) The process of reprogramming cannot take place with the IC in the circuit. The EPROM IC must be removed from the circuit and the stored program can be erased by exposing the memory cells to ultraviolet light through a "window" on the IC package. This process takes about half an hour.

10.4.13 Electrically Erasable Programmable ROM (EEPROM)

Another type of reprogrammable ROM device is EEPROM (Electrically Erasable Programmable ROM), which is also known as Electrically Alterable Programmable ROM (EAPROM). The EEPROM overcomes the disadvantages of EPROM. EEPROM

can be erased and programmed by the application of controlled electric pulses to the IC in the circuit, and thereby changes can be made in the selected memory locations without disturbing the correct data in other memory locations. EEPROM is non-volatile like EPROM but does not require ultraviolet light to be erased. The non-volatility of EEPROM permits a system to be immune to power interruptions.

EEPROM is a rugged, low power semiconductor device and it occupies less space. It has the advantages of program flexibility, small size and semiconductor memory ruggedness, i.e. low voltages and no mechanical parts. The requirement of low power supports field programming in portable devices for communication encoding, data formatting and conversion, and program storage. With EEPROM, the programs can be altered remotely, possibly by telephone.