

Objective Que. & Ans. Test-1

Sub:- DC

Branch - ECE, 4<sup>th</sup> sem.

Que:-1 How many 2:1 MUX are required to generate 2<sup>n</sup>:1 MUX?  
(a) 2<sup>n</sup> (b) 2<sup>n</sup> - 1 (c) 2<sup>n</sup> + 1 (d) 2<sup>n-1</sup>

Que:-2 What is the number of select lines required in 1:n DE-MUX?

(a) 2 (b) n (c) 2<sup>n</sup> (d) log<sub>2</sub> n

Que:-3 How many 2:1 MUX is required to realize 2-input Ex-OR logic gate?

(a) 1 (b) 2 (c) 3 (d) 4

Que:-4 In expression (A+BC), the total number of minterms?

(a) 2 (b) 3 (c) 4 (d) 5

Que:-5 How many 4:1 MUX are required to generate 512:1 MUX?

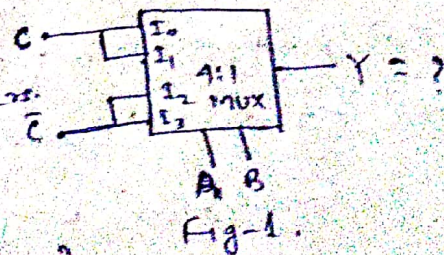
(a) 172 (b) 171 (c) 169 (d) 170

Que:-6 When two 4-bit parallel address are cascaded, we get  
(a) 4-bit (b) 8-bit (c) 16-bit (d) 17-bit ; parallel address.

Que:-7 Look ahead carry is used to make adder —

(a) slower (b) faster (c) Minimize logic gates (d) None of these.

Que:-8 Boolean function of logic ckt shown in fig-1 is: Y = ?



Que:-9 "ASCII" Code has ..... characters.

Que:-10 Minimum No. of NAND gates realize to Ex-OR gate is .....

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