ADDER and Subtractor
(Combinational circuit)

There are two types of digital circuits as following :-

i) Combinational circuit
ii) sequential circuit.

i) <u>Combinational digital circuit</u> :- When logic gates are connected together to obtain or produce specific output for a certain specified combinations of inputes with no storage element or memory, is called combinational circuit. In other word, the digital ckt, in which output depends upon only present value of input combination not on past value, is called combinational circuit. Adder, Subtractor, MUX, DE-MUX, Decoder, Encoder etc are combinational digital ckt. A basic block diagram of combinational ckt is given below —

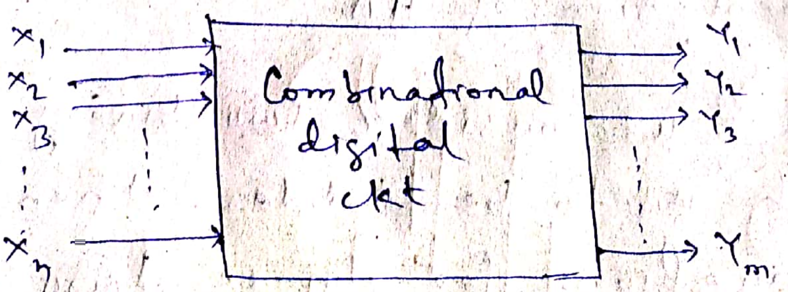


Fig-1.

Adder circuit

A combinational circuit which add the binary bits, is called Adder. There are following types of Adders —

i) Half-Adder
ii) Full-Adder.

i) **Half-Adder:**– A combinational digital circuit which add two 1-bit binary number and produces two outputs as sum (Σ) and output carry (C_o), is called Half-Adder. It is obvious, that, a Half-Adder has two inputs and two output lines. The fig-2 given below represents a basic block diagram of Half-Adder.

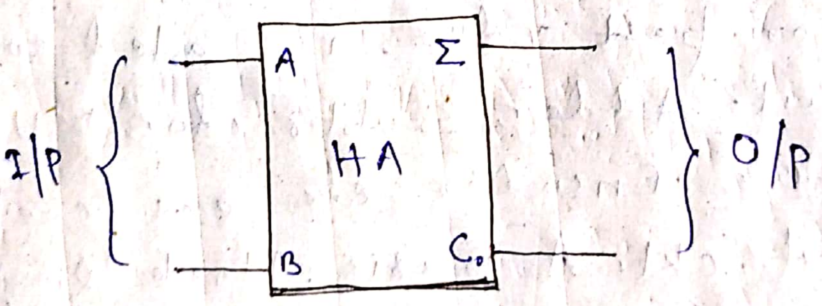


Fig-2.

Implementation of HA

Let, us consider, two binary bits A and B which is to be added, then possible combinations for these two variables and sum and carry can be observed from truth table-1 shown in fig-3.

Table - 1.

A	B	Σ	C_o
0	0	0	0
0	1	1✓	0
1	0	1✓	0
1	1	0	1✓

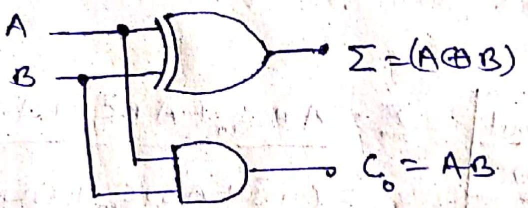
Fig - 3.

Standard SOP corresponding to Σ is $\bar{A}B + A\bar{B}$

and " " " " C_o is AB

$$\therefore \Sigma = \bar{A}B + A\bar{B} = (A \oplus B)$$

$$C_o = AB$$



Half-Adder.

Fig - 4. (a)

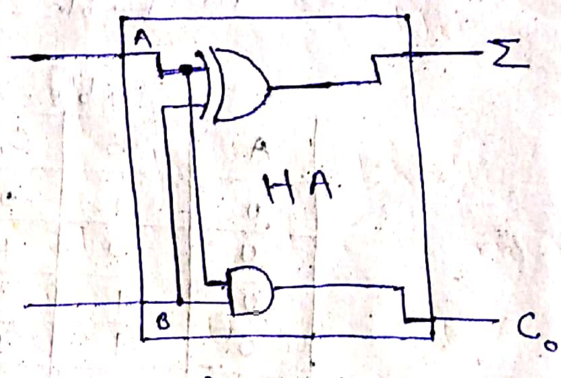


Fig - 4(b)

ii) Full-Adder :- A combinational circuit which performes addition of three binary bits and produces two outputs as Sum (Σ) and carry-out (C_{out}) is called full-adder. It is clear, that, a full-adder has three inputs and two output lines. A basic block diagram is shown in fig - 5

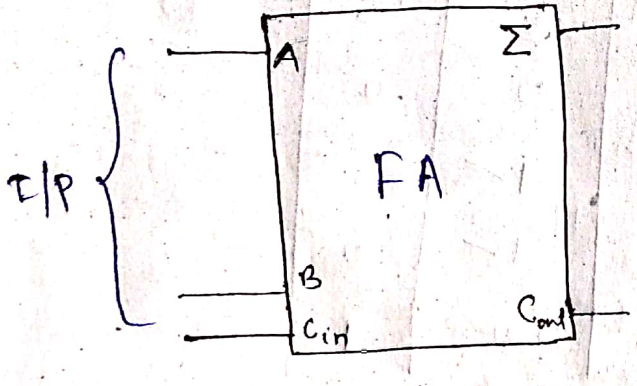


Fig-5

Implementation of FA

It is clear, that a full-adder has three inputs as two binary bits and carry input. The possible combinations can be listed as in table-2, Fig-6

Table-2.

A	B	C_{in}	Σ	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig-6.

$$\Sigma = \bar{A}\bar{B}C_{in} + \bar{A}B\bar{C}_{in} + A\bar{B}\bar{C}_{in} + ABC_{in}$$

$$= (\bar{A}\bar{B} + AB)C_{in} + (\bar{A}B + A\bar{B})\bar{C}_{in}$$

$$= \overline{(A \oplus B)}\, C_{in} + (A \oplus B)\bar{C}_{in}$$

or, $\Sigma = (A \oplus B) \oplus C_{in}$

And,

$$C_{out} = \bar{A}BC_{in} + A\bar{B}C_{in} + AB\bar{C}_{in} + ABC_{in}$$

$$= (\bar{A}B + A\bar{B})C_{in} + AB(\bar{C}_{in} + C_{in})$$

or, $C_{out} = (A \oplus B)C_{in} + AB$

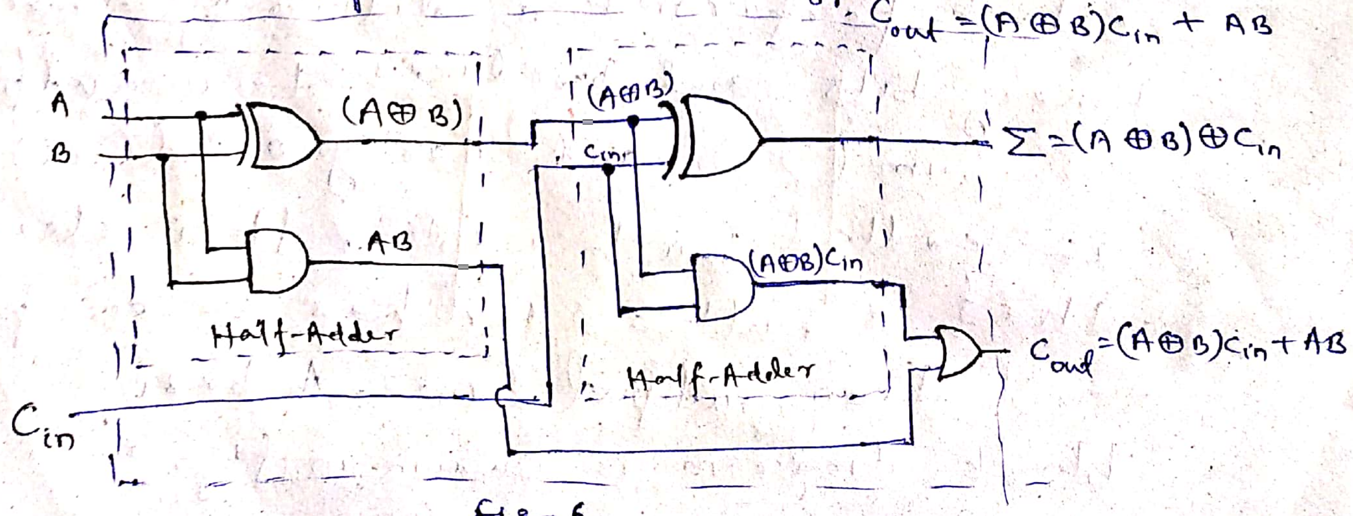
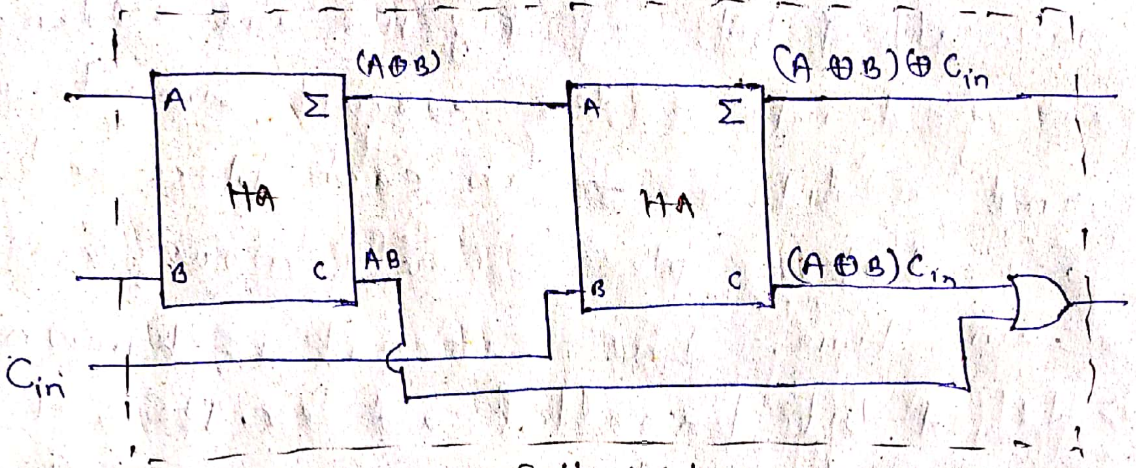


Fig-6



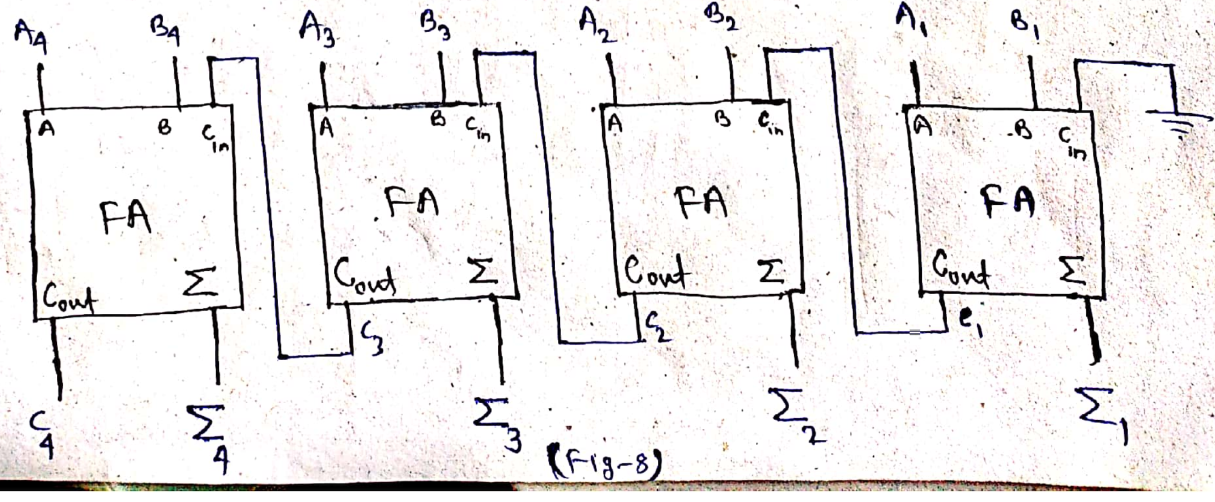
Full-Adder using two HA

Fig-7.

4-bit Parallel Adder

A full adder is capable to add only two bits of a binary numbers along with a carry input. But, in practice, we need to add binary numbers with large number of bits. For this purpose, we design parallel adder.

A group of 4-bits is called nibble. To add ~~4-bits~~ two 4-bit binary numbers, we can use 4-full adder connected parallely in such a way that the carry out of LSB stage is fed to the carry-in of next MSB stage as shown in fig-8



(Fig-8)

Since, all 4-bits of augend and addend are fed into adder circuit simultenously and addition ~~of~~ in each place or position are taking place simultaneously or at same time, the circuit is known as 4-bit parallel adder. Here, it is to noted that, the sum and output carry of any stage cannot be produced untill input carry occurs. This causes a time delay.

Propagation delay: The carry propagation delay is defined as the time elapsed or taken by a full adder from application of carry-input to produce the carry output.

SUBTRACTOR

A combinational digital ckt that can subtract two binary bits, is called Subtractor. There are following two types of subtractors —

i) Half-wave subtractor
ii) Full-wave subtractor.

i) **Half-wave subtractor** : A subtractor which having two inputs and produces difference of supplied binary bits and produces two outputs as difference D and borrow B, is called Half-subtractor. If X is minuend and Y is subtrahend bit, then, their possible combination of subtraction can be observed from truth table-3.

Table-3

X	Y	D	B
0	0	0	0
0	1	1✓	1✓
1	0	1✓	0
1	1	0	0

Fig-9

Standard SOP for D is $\bar{X}Y + X\bar{Y}$

" " " B is ~~$\bar{A}B$~~ $\bar{X}Y$

i.e, $D = \bar{X}Y + X\bar{Y} = \cancel{(A \oplus B)}\ (X \oplus Y)$

$B = \cancel{\bar{A}B}\ \bar{X}Y$

Logic circuit implementation —

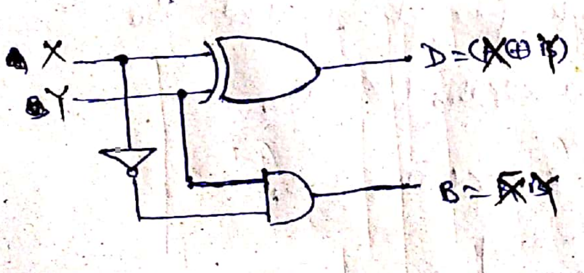


Fig-10(a)

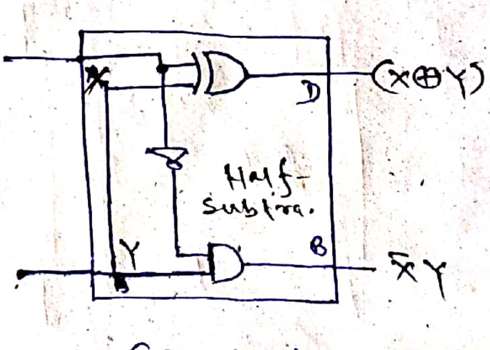


Fig-10(b)

ii) <u>Full-subtractor</u> :- A combinational circuit which performes a subtraction between two bits taking into account the borrow of lower significant stage, and produces two output as difference D and borrow-out B_o is called full-subtractor. Fig-11. shows a block diagram of Full-subtractor.

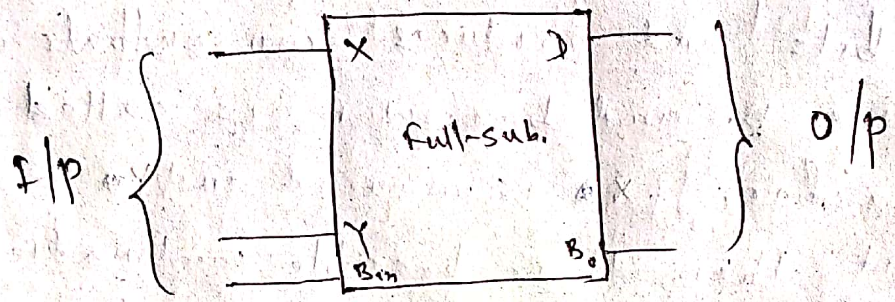


Fig-11

A truth table for the illustration of full-subtractor is shown in table-4.

Table-4

X	Y	B_{in}	D	B_o
0	0	0	0	0
0	0	1	1✓	1
0	1	0	1✓	1
0	1	1	0	1
1	0	0	1✓	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1✓	1

Fig-12.

Standard SOP for D —

i.e, $D = \bar{X}\bar{Y}B_{in} + \bar{X}Y\bar{B}_{in} + X\bar{Y}\bar{B}_{in} + XYB_{in}$

or, $D = (\bar{X}\bar{Y} + XY)B_{in} + (\bar{X}Y + X\bar{Y})\bar{B}_{in}$

$= (\overline{X\oplus Y})B_{in} + (X\oplus Y)\bar{B}_{in}$

or $\boxed{D = (X\oplus Y)\oplus B_{in}}$

Similarly, standard SOP for Borrow B_o is —

$B_o = \bar{X}\bar{Y}B_{in} + \underline{\bar{X}Y\bar{B}_{in} + \bar{X}YB_{in}} + XYB_{in}$

$= (\bar{X}\bar{Y} + XY)B_{in} + \bar{X}Y(\bar{B}_{in} + B_{in})$

or $\boxed{B_o = (\overline{X\oplus Y})B_{in} + \bar{X}Y}$

Implementation by logic gate

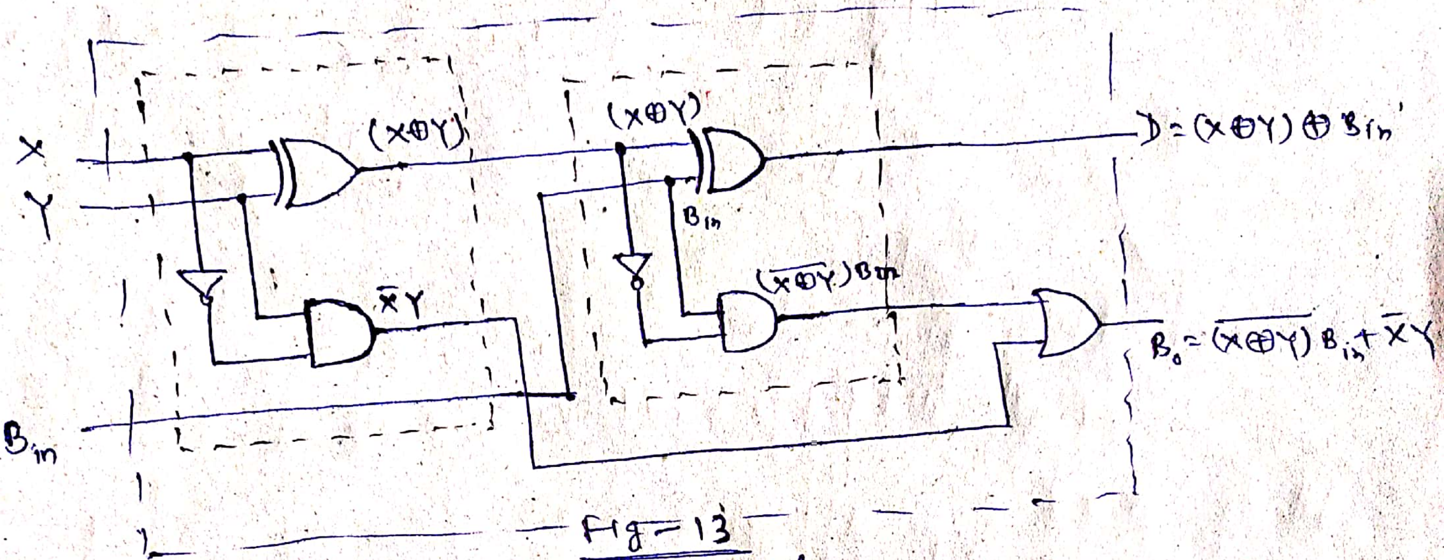


Fig-13
full-subtractor.

Block diagram