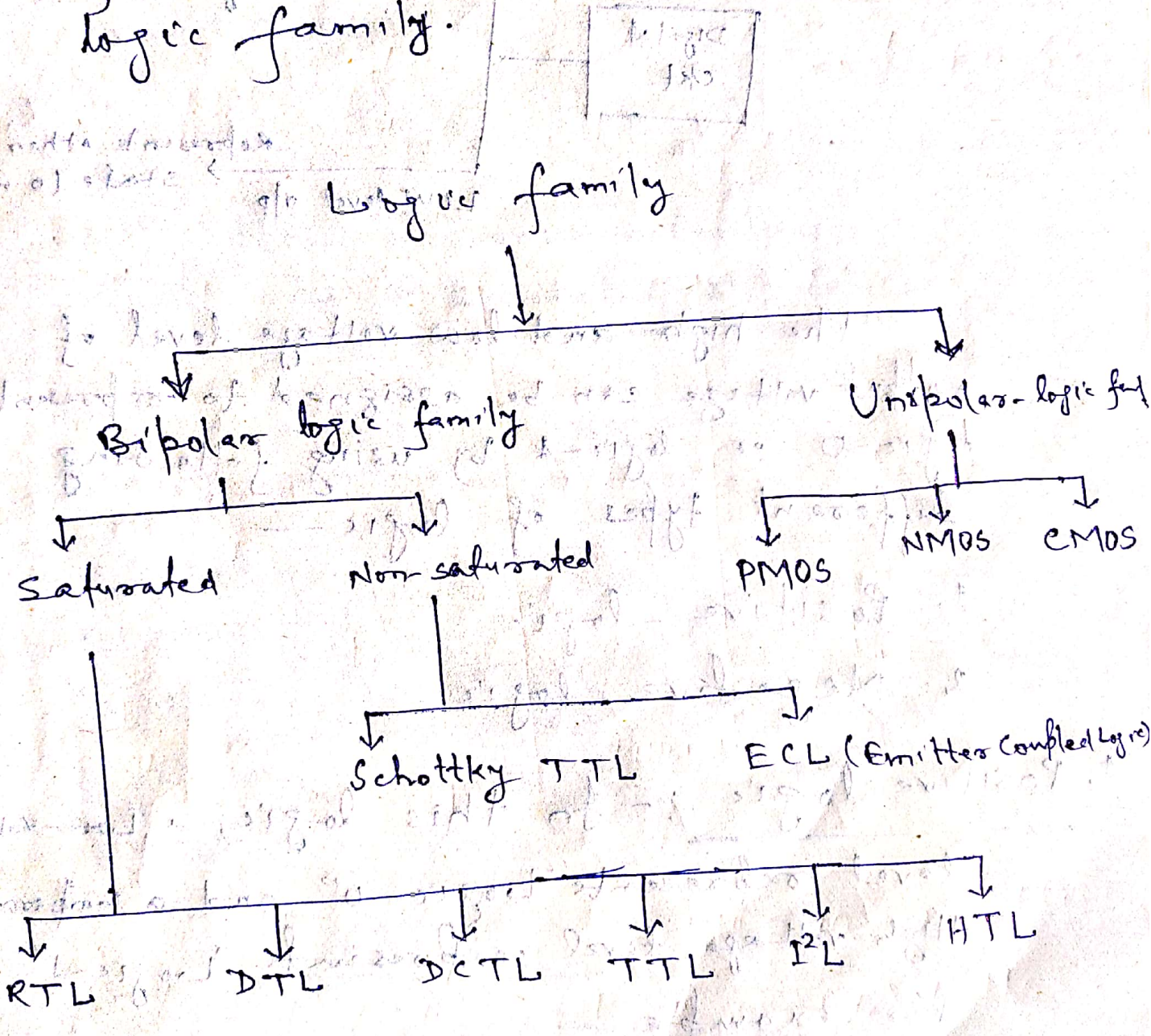
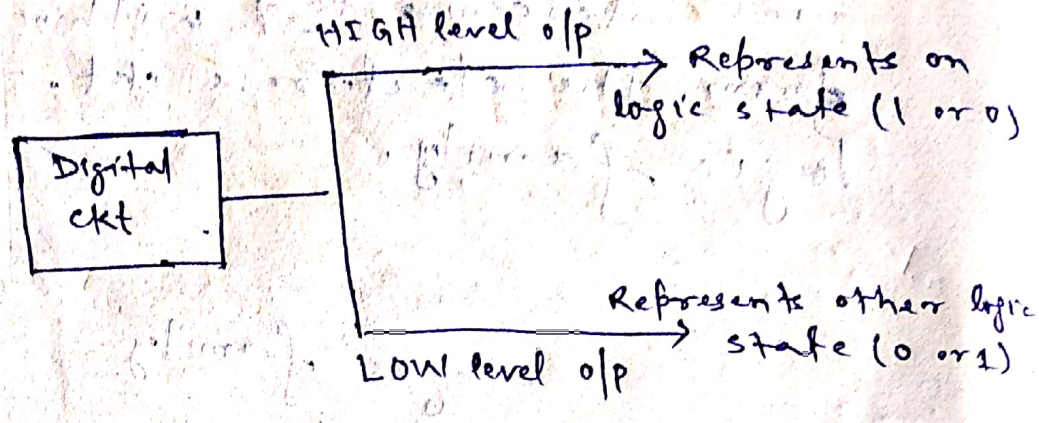
Logic families

Logic gates and memory devices are fabricated as Integrated circuit (IC) because, Diode, Transistor, MOSFET etc are the internal parts of ICs. The various components are interconnected within the chip to form the electronic ckt. They are called logic family.



(2) # Logic levels

Digital circuit has only two distinct output voltage levels. These two voltage levels are used to represent logic-0 and logic-1.



The high and low voltage level of output voltage can be assigned to represent logic-0 or logic-1 by using following different types of logic —

1. Positive - logic
2. Negative - logic

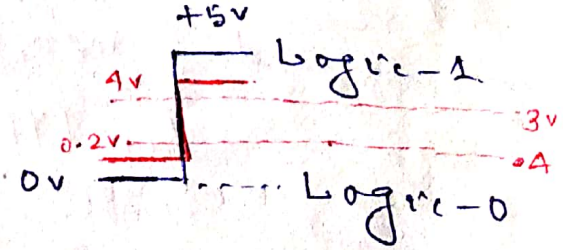
1. **Positive logic** :- In this logic, a Low-voltage level represents "Logic-0" and a comparatively High voltage level represents "Logic-1"

For example —

Positive logic

Logic-0 ≡ 0volt

Logic-1 ≡ +5 volt



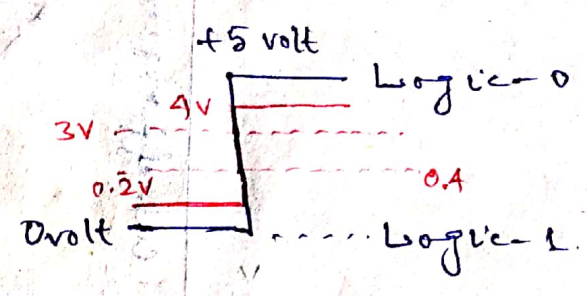
2. Negative Logic :- In this logic, a low-level voltage represents Logic-1 and comparatively High voltage represents Logic-0.

Page-3

Example —

Logic-0 ≡ +5 volt

Logic-1 ≡ 0 volt



How a transistor functions as a switch (NOT gate) ?

Let us consider a transistor with some specifications as —

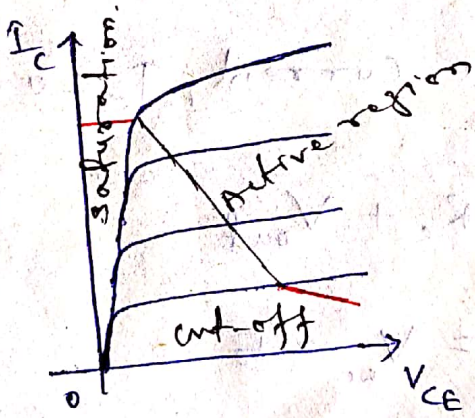
$R_c = 1\ K\Omega$

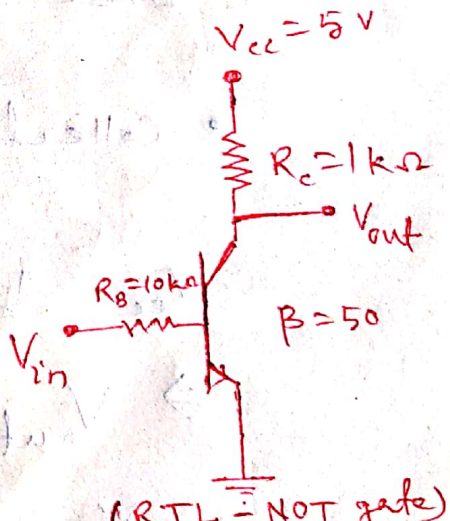
$R_B = 10\ K\Omega$

$V_{CE_{sat}} = 0.2V$

$V_{BE_{sat}} = 0.7V = V_{BE_{on}}$

$\beta = 50$





(RTL - NOT gate)

Fig-1.

The switching behaviour of transistor can be analysed with graphical approach in their, Cut-off → Active → saturation region.

Pg-4

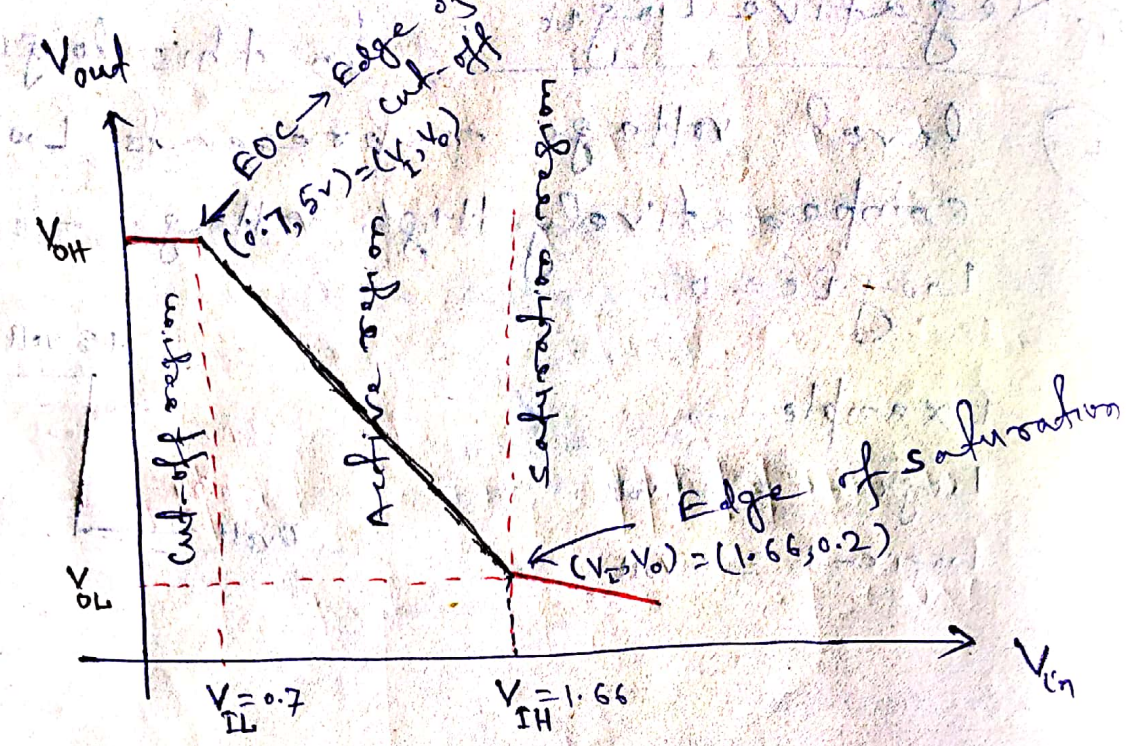
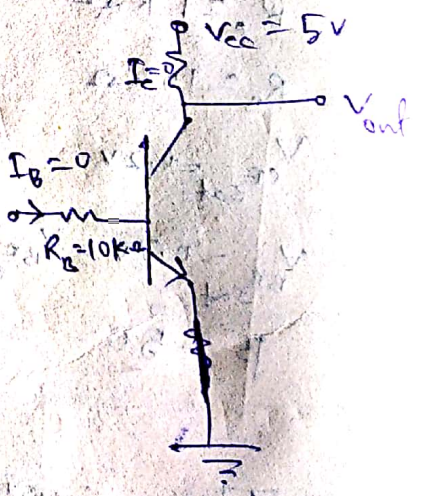


Fig-3.

case:-I. Cut-off region

When transistor is in cut-off,

- Base current, $I_B = 0$, $V_{BE} < 0.7 \Rightarrow V_{in} < 0.7$
- Collector current, $I_C = 0$



$$V_{cc} = I_C R_c + V_{out}$$

$$\Rightarrow V_{out} = V_{cc} = 5$$

$$V_{out} = 5 \text{ volt.}$$

i.e

Input Logic LOW, then output Logic HIGH

Case:-II Active region

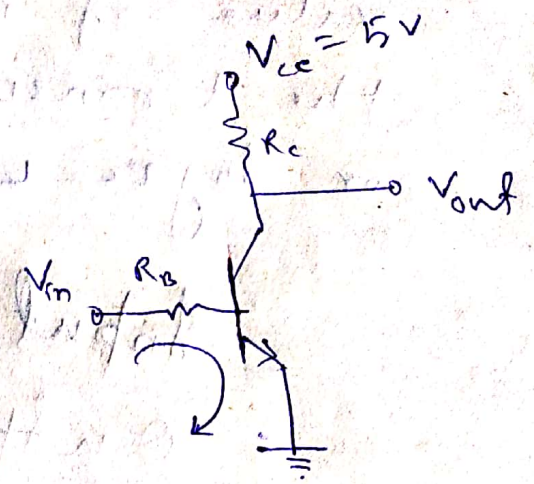


Fig-4.

- $V_{in} = I_B R_B + V_{BE_{on}}$

  or $I_B = \dfrac{V_{in} - V_{BE_{on}}}{R_B}$

- $I_c = \beta I_B$

Here $V_{CE} < V_{CE_{sat}}$

- $V_{out} = V_{cc} - I_c R_c = V_{cc} - \beta I_B R_c$

$$\Rightarrow V_{out} = V_{cc} - \beta R_c \left(\frac{V_{in} - V_{BE_{on}}}{R_B} \right)$$

Case:-III Saturation region

- V_{in} (or I_B) increases, second transition point (from fig-3) is reached when $V_{out} = V_{CE_{sat}}$

- $I_{C(EOS)} = \dfrac{V_{cc} - V_{CE_{sat}}}{R_c} = \dfrac{5 - 0.2}{1 \times 10^3} = 4.8\,mA$

- $I_{B(EOS)} = \dfrac{I_{C(EOS)}}{\beta} = \dfrac{4.8}{50} = 0.096\,mA$

- $V_{in(EOS)} = I_{B(EOS)} R_B + V_{BE_{on}} = 0.096 \times 10 + 0.7 = 1.66\,V$

- That is, if $V_{in} \geq 1.66\,V$, transistor goes to saturation and output is Logic-LOW.

(6) In other word, 1.66 volt is minimum value of input voltage to turn the transistor into saturation or logic-LOW output. i.e When

Input logic - HIGH
Output - logic - LOW

Thus, Here we see that, transistor functions as a NOT gate switch in cut-off & saturation region.

Here,

V_{IL} = Maximum input voltage so that transistor remains in cut-off (Output - Logic - HIGH) and treated as input logic - LOW = 0.7v

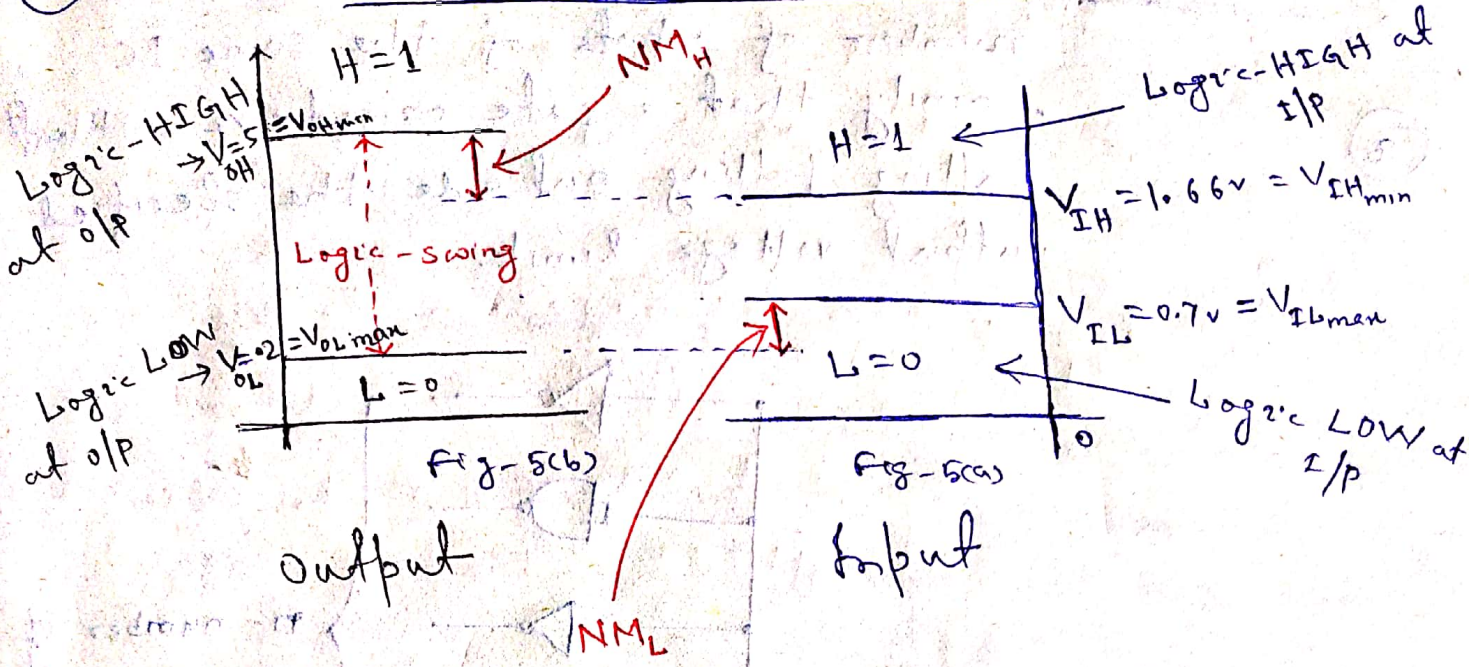
V_{IH} = Minimum input voltage which turns the transistor into saturation (Output - logic - LOW) and treated as input - logic - HIGH.

V_{OL} = This is the max^m output voltage which will be considered as logic-LOW output.

V_{OH} = Min^m value of o/p voltage considered as Logic-HIGH o/p

(7)

Input-Output Mapping



Logic swing $= V_{OH} - V_{OL} = 5 - 0.2 = 4.8\,v$

NM_L = Noise Margin LOW $= V_{IL} - V_{OL} = 0.7 - 0.2 = 0.5\,v$

NM_H = Noise Margin HIGH $= V_{OH} - V_{IH} = 5 - 1.66 = 3.34\,v$

Some Terminology

 # Fan-in :- The number of inputs to a gate without any degradation of its voltage level is called fan-in. For example, a two-input gate will have a fan-in equal to 2.

(8)

Fan-out :- Fan-out is defined as the max^m number of inputs of the same IC family that a gate can drive without falling falling out-side the specified output voltage limits.

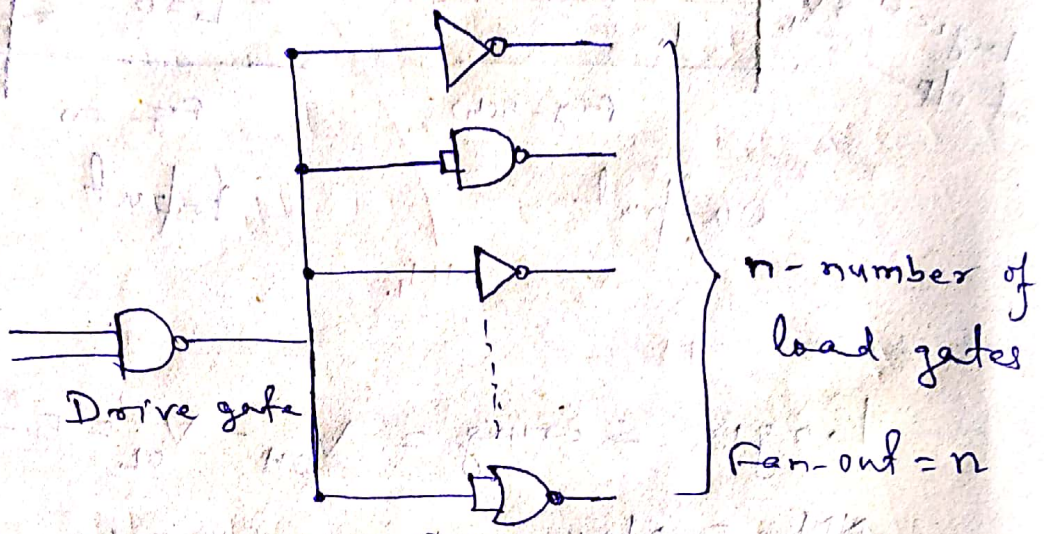


Fig-6

For, example, a fan-out of 5 indicates that, the gate can drive (supply current to) at most 5-inputs of the same IC. Fan-out is also called loading factor.

Noise Margin :- Noise Margin or Noise immunity is defined as the ability of a logic circuit to tolerate the noise without causing any unwanted change in the output. A quantitive measure noise immunity is called noise margin.

High-Level noise margin = $NM_H = V_{OH} - V_{IL} = V_{OH_{min}} - V_{OL_{max}}$

Low-level noise margin = $NM_L = V_{IL} - V_{OL} = V_{IL_{max}} - V_{OL_{max}}$

Propagation Delay :- The output of a logic gate does not change its state instantaneously in response to the change in the state of its input. There is always, a time delay between these two events, which is called propagation delay.

(9)

Thus, propagation delay is defined as time delay bet^n the instant of application of an input pulse and the instant of occurrence of corresponding output pulse.

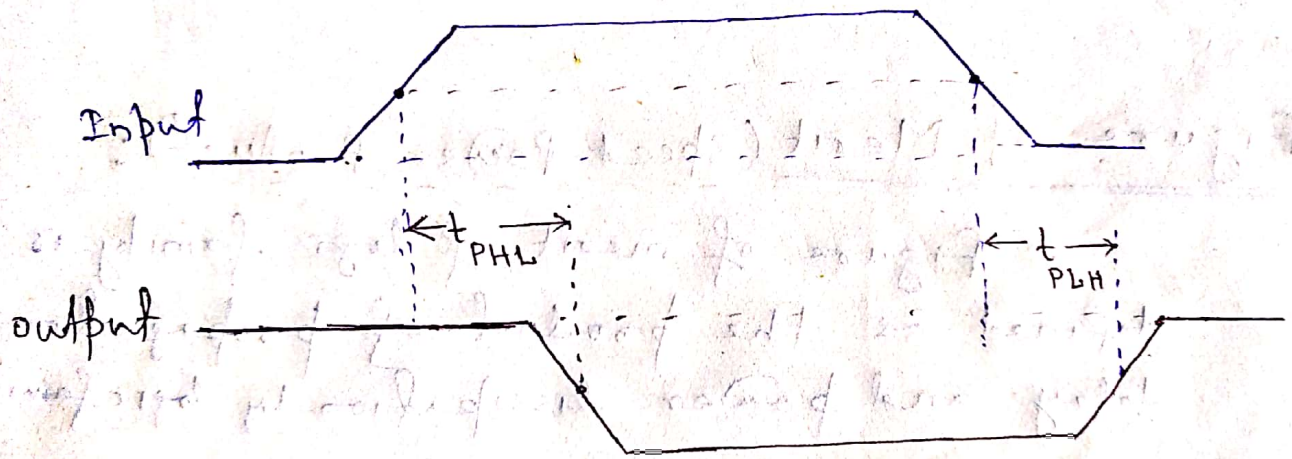


Fig-7. : Propagation delay. (for NOT gate)

Propagation delay is measured bet^n 50% voltage level of input and output waveform as illustrated in fig-7.
Propagation delay can be studied in following category —

(10)

ii) t_{PHL} : The propagation delay measured when output is making a transition form HIGH (1) to LOW (0) state

iii) t_{PLH} : The propagation delay measured when output is making a transition from LOW (0) to HIGH (1) state.

Figure of Merit (Speed-Power Product):

Figure of merit of logic family is defined as the product of propagation delay and power dissipation by logic family.

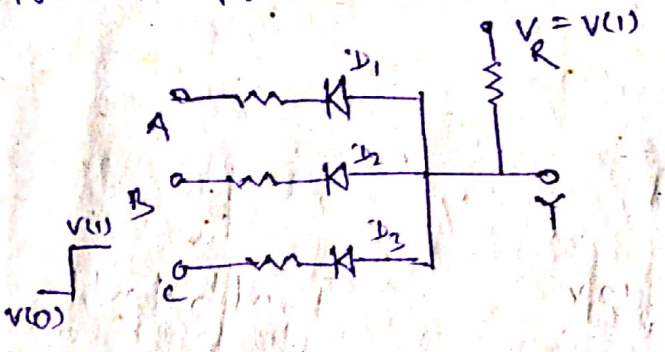
> Figure of merit = Prop. delay × Power dissipat

In practice figure of merit should be as low as possible. Figure of merit is always ~~compromise~~ compromise bet^{n} speed and power-dissipation. That means if we try to reduce propagation delay, power dissipation will increase and vice-versa.

DTL (Diode-Transistor Logic)

DTL belongs to the saturated bipolar logic family.

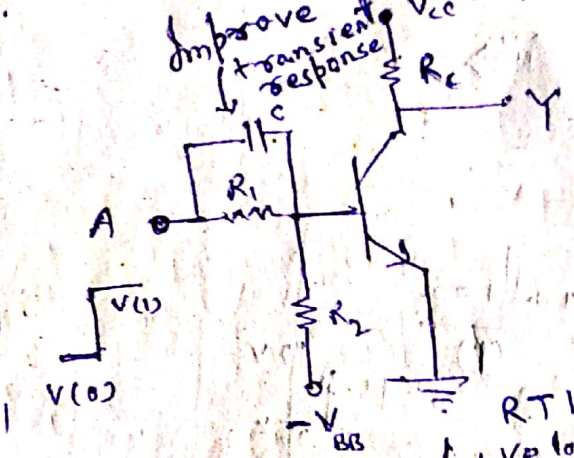
Diode-ON = forward bias = 0 volt



(+ve logic AND gate)

(Fig-1)

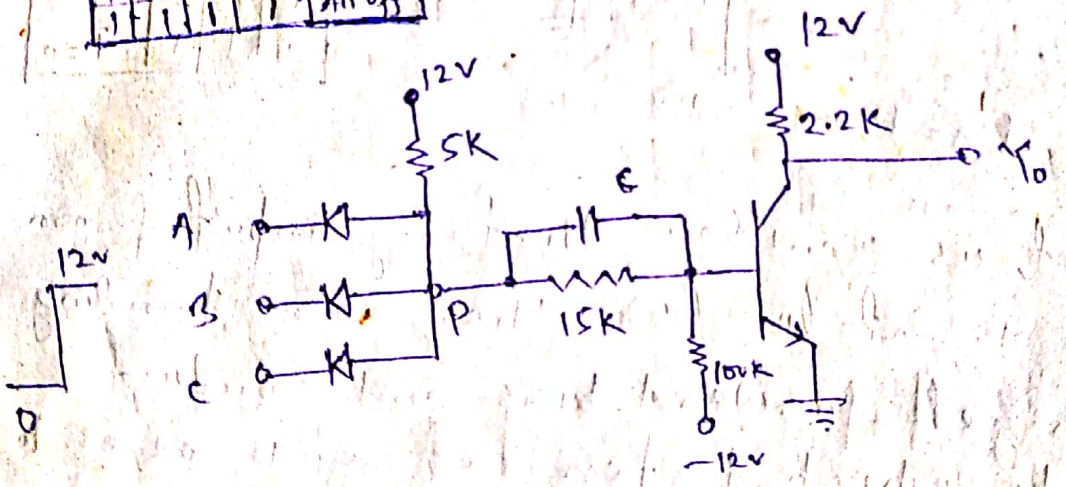
A	B	C	Y	Diode ON
0	0	0	0	D_1, D_2, D_3
0	0	1	0	D_1, D_2
0	1	0	0	D_1, D_3
0	1	1	0	D_1
1	0	0	0	D_2, D_3
1	0	1	0	D_2
1	1	0	0	D_3
1	1	1	1	All off



RTL (+ve logic NOT gate)

Fig-(2)

A	Y	Transistor act
0	1	Off, HIGH
1	0	Saturation LOW



DTL – Fig (3) – (Three-input NAND gate)

The fig (3) shows a Diode Transistor logic which is the combination of an +ve logic AND gate and NOT gate. We have to

1) ~~verify~~ verify that the ckt of fig-(3) is a +ve NAND (AND+NOT) for the binary level 0-12V.

iii) If drop across a conducting diode is 0.7v and the sum of source and diode resistance is 1k, is the NAND logic satisfied?

Explanation

(I)

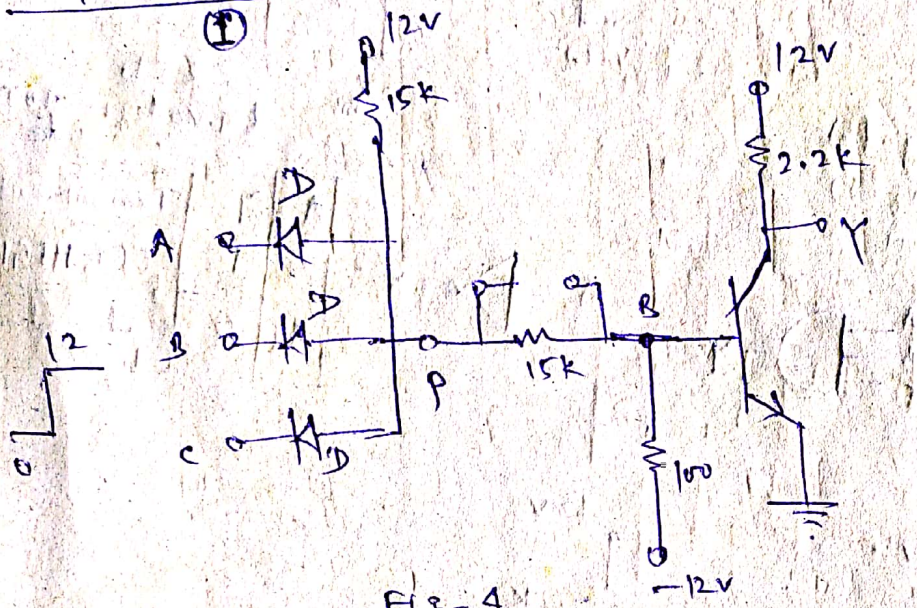
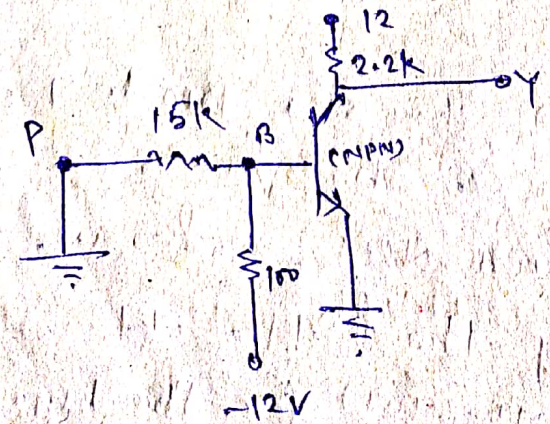


Fig-4

Truth table

A	B	C	Y
0	0	0	$\bar{0}=1$
0	0	1	$\bar{0}=1$
0	1	0	$\bar{0}=1$
0	1	1	$\bar{0}=1$
1	0	0	$\bar{0}=1$
1	0	1	$\bar{0}=1$
1	1	0	$\bar{0}=1$
1	1	1	$\bar{1}=0$

Case:-I Let, us consider that any input from A, B, C is at low (0) then corresponding diode gets forward bias and conduct due to which potential at P rises to '0'. In this case ckt can be redrawn as below -



V_B = Voltage drop across 15kΩ. ——— (1)

$= \frac{-12}{115} \times 15 = \frac{-180}{115}$

$= -1.56$ volt

Fig-(2)

-ve voltage of base indicates that base-emitter junction is reverse biased and transistor is in cut-off. Hence, output $Y = V_{ce} = HIGH$ which satisfied the condition to perform NAND operation.

Case-II. If all the inputs are at HIGH.

for this case all input diodes are reverse biased and potential at P is not now 0. ckt can be redrawn as below ——

Here we assum diode forward resistence and assumed to be zero.

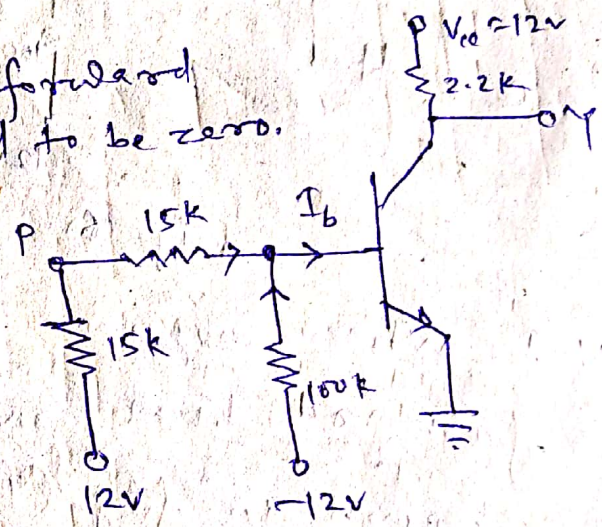


Fig-⑥

Then,

$V_B = 0$

$$I_b = \frac{12-0}{30} + \frac{-12-0}{100}$$

$$= \frac{12}{30} - \frac{12}{100} = 0.40 - 0.12$$

$$= 0.28\,mA$$

from output side, when transistor is at saturation region ——

$$I_c = \frac{12}{2.2}$$ [Neglecting Collector saturation resistance if it is not so then $V_{CE,sat} = 0.2V$]

$$\therefore I_c = 5.45\,mA$$

$$\therefore \beta_{min} = h_{FE_{min}} = \frac{I_c}{I_B} = \frac{5.45}{.28} = 19.48$$

i.e if $\beta \geq 19$, transistor will be at Saturation and in this case output $Y = 0$ which desired cond^n for NAND gate.

2) If drop across conducting diode is considered as 0.7v and sum of diode forward and source resistance 1KΩ.

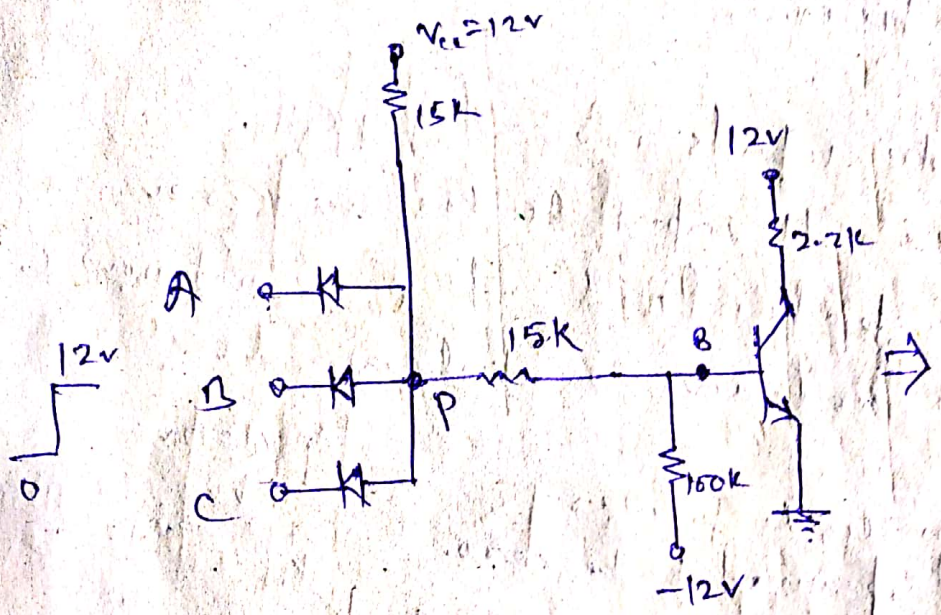


Fig-7(a)

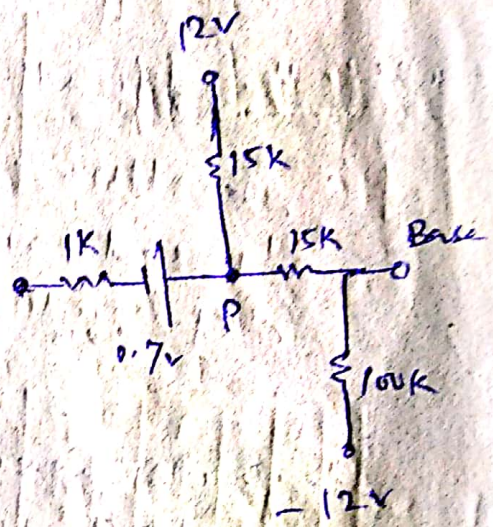


Fig-7(b)

Case:-I When any one input at low, diode become forward bias and ckt may drawn as shown in fig-(7).

Now,

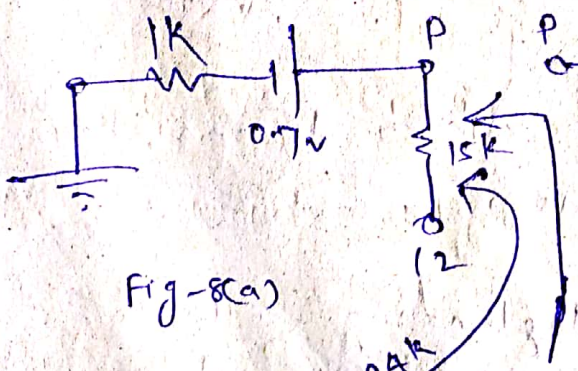


Fig-8(a)

$R_{th} = 1 \| 15 = \frac{15}{16} = 0.94K$

$V = V_{01} + V_{02}$ = By superposition

$= \frac{0.7}{16} \times 15 + \frac{12}{16} \times 1$

$= \frac{10.5}{16} + \frac{12}{16} = \frac{22.5}{16} = 1.40625$

$= 1.41$ volt.

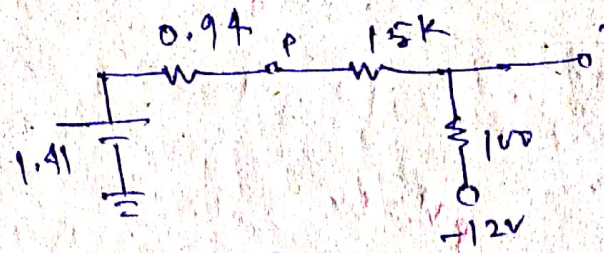


Fig-8(b)

Now,

V_B = By superposition.

$$= \frac{1.41}{115.94} \times 100 + \frac{-12}{115.94} \times 15.94 = -0.44V$$

-ve potential at base of NPN transistor makes base as reverse biased and hence diode (Transistor) is off, and output becomes $Y = V_{cc} = 5V$ treated as HIGH.

case:- II When all inputs are at HIGH, all input diodes, are reverse biased and hence, operation will be the same as that of fig-(5) explanation.

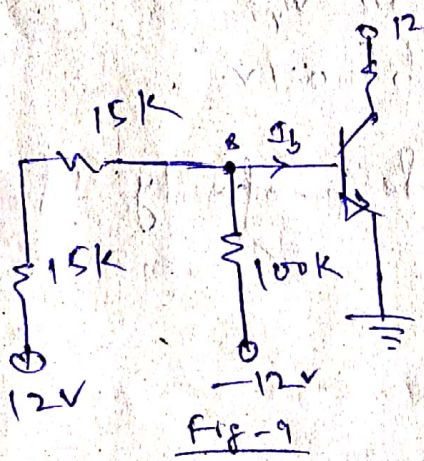


Fig-9

$$I_b = \frac{12-0}{30} + \frac{12-0}{100} = 0.28mA$$

$$I_c = \frac{12}{2.2} = 5.45$$

$$\beta = \frac{5.45}{0.28} = 19.04$$

If $\beta \geq 19$, then transistor saturates and output results as 0. Thus, from above all discussion, we conclude that ckt(fig-3) DTL is NAND logic.