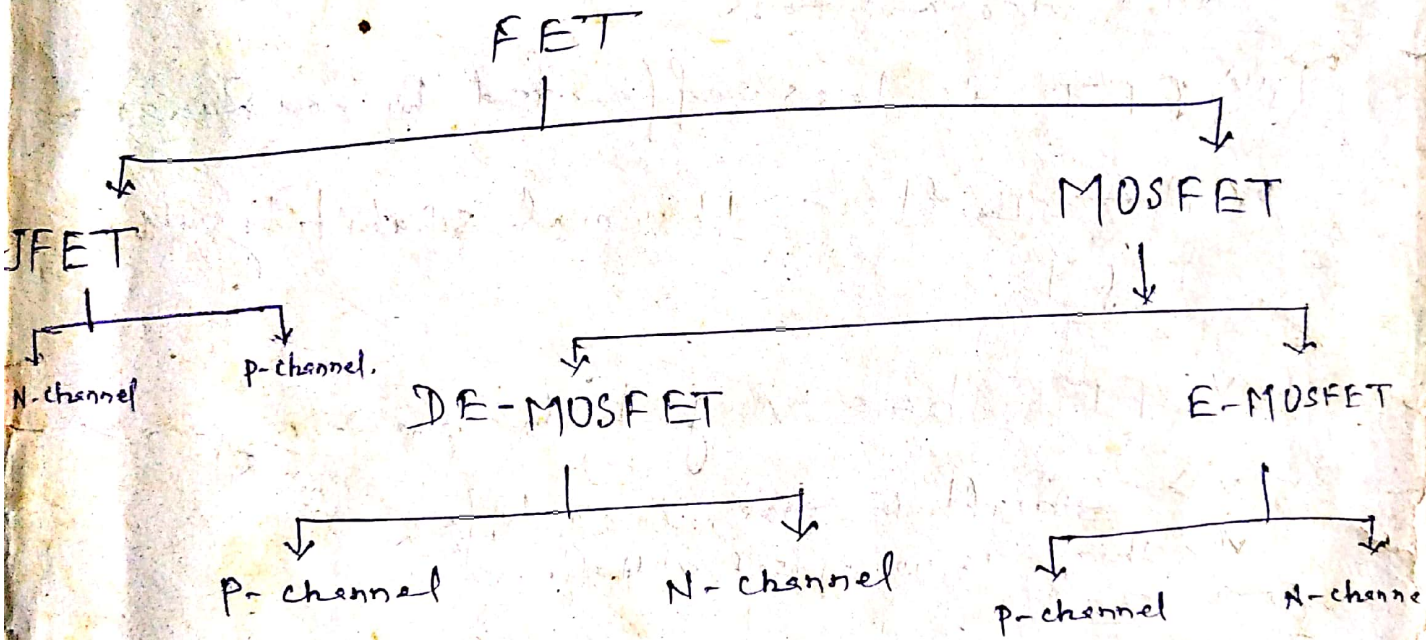
FET (Field Effect transistor)

FET is a three terminal unipolar semiconductor device, in which the current is controlled by an electric field. Basically there are two types of FET ——

i) JFET (Junct" Field Effect transistor)

ii) MOSFET (Metal-Oxide-semiconductor FET) (or IGFET → Insulated gate FET).



dvantages of FET over Conventional transistor :→

i) FET is a unipolar semiconductor device, depending only upon the majority carrier (either electrons or holes) where as BJT depends upon both the carriers majority and minority. Vacuume tube is also a unipolar device. i.e in FET the

ii) Current conduction is due to only one type of carrier (either electrons or holes).

(2) ii) FET has high input impedance. For ord. FET offers a very high input impedance of order 100MΩ and for MOSFET of 10^{10} to 10^{15} Ω. Thus, FET is voltage contro device like the vacuum-tube where as BJT is a current controlled device.

iii) FET is less noisy than the vacuum-tube and transistors.

iv) FET is less affected by radiation

v) ~~Bet~~ Better thermal stability than th BJT.

vi) FET has very high power gain.

vii) Small in size, long life,

viii) there is no offset voltage

Comparision.

FET	BJT
i) Unipolar device	i) Bi-polar device
ii) Current conduction takes place due to only one carriers (Either electrons or holes) (Majority carriers)	ii) Current-conduct takes place due to bo the carriers, majori and minority carri
iii) Voltage-controlled device	iii) Current-control device.
iv) High-input impedance. due to reverse bias.	iv) Low input impedan than FET.

(3) v) Gain is characterised by B. trans conductance	v) Gain is characterised by voltage gain.
vi) Better thermal stability	vi) Less thermal stability
vii) Transconductance is low and hence voltage gain is low.	vii) Transconductance is high and hence voltage gain is high.

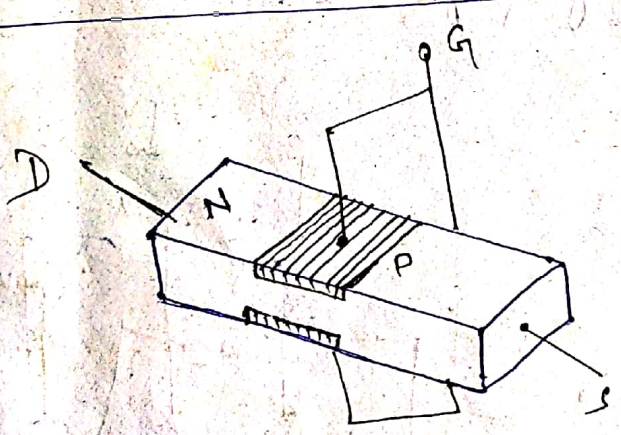
Input resp. high, $V_i \rightarrow$ High, $g_m = \frac{I_o}{V_i} \rightarrow$ Low.

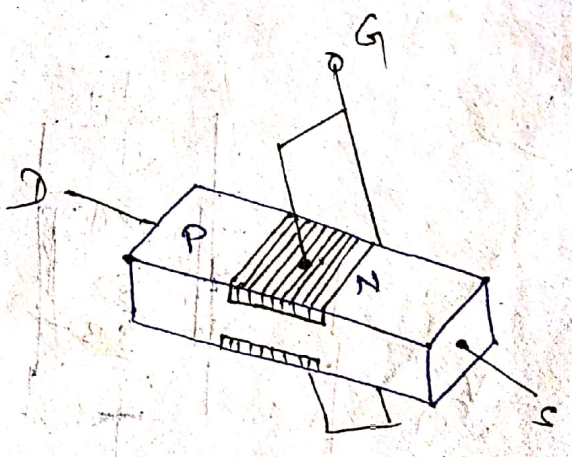
Disadvantage :- i) Costly

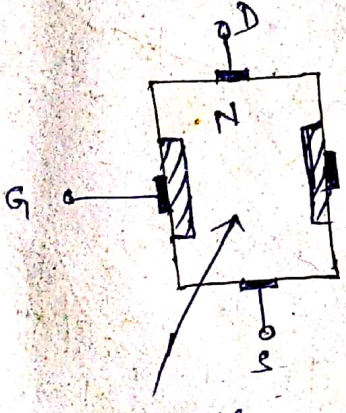
ii) Voltage gain is low.

iii) FET has relatively small gain BW product.

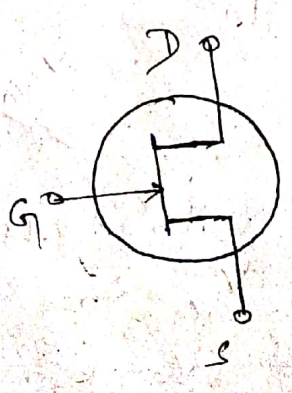
Basic construction



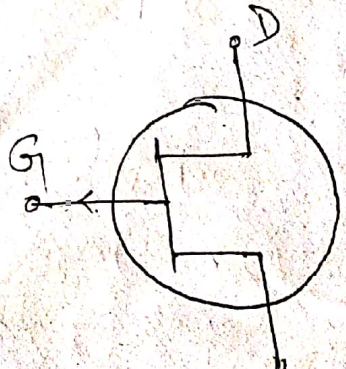




N-channel



N-channel



P-channel

(4) A FET has the following terminal notat

i) Source :→ It is the terminal through which majority carriers enters into the bar.

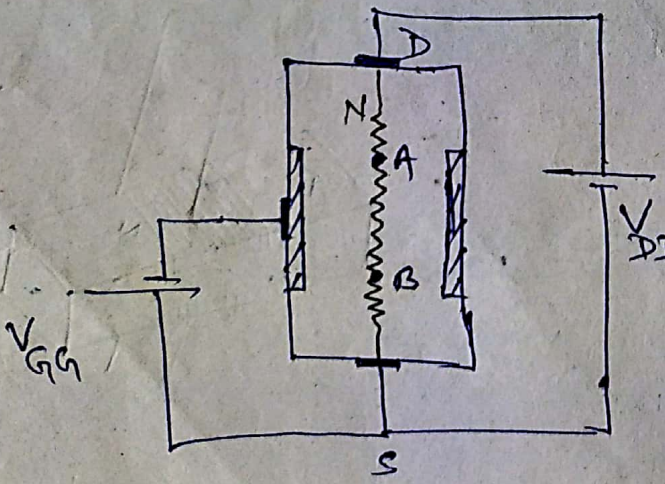
ii) Drain :→ It is the terminal through which majority carriers leave the bar.

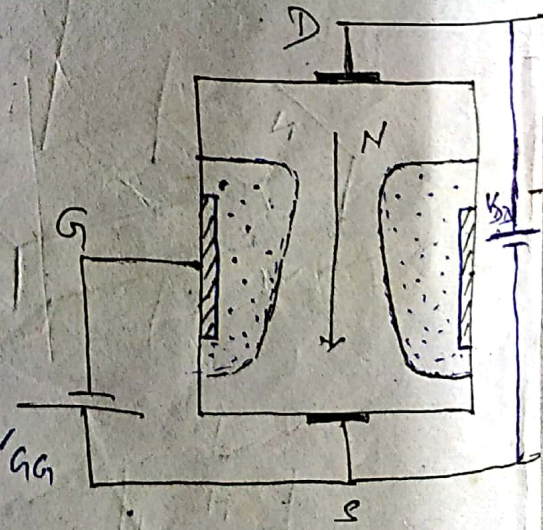
iii) Gate :→ These are the heavily doped impurity regions which are internally connected and form two p-n junctions.

iv) Channel :- The space bet" the two gates thro which majority carriers pass.

Operation of "FET"

To understand the operation of FET, we Consider the following fig-1 & 2.





Let, first consider that the gate reverse bias voltage (battery) V_{GG} and Drain supply V_{DD} are not Connected. We know that there exis a space charge region on either side

(5) of P-N junct°. Now, let V_{DD} is connected across Drain and source keeping V_{GG} disconnected. This voltage drop V_{DD} bet° drain and source uniformally ~~dec~~ decreases while going from drain to ~~source~~ source. Let this voltage drops through a ~~channel res~~ N-channel (fig-1) resistance (R_{DS}). Clearly, the voltage drop near the drain is higher then the drop near source. Let, A and B are two points near drain and source respectively as shown in fig-1. clearly $V_A > V_B$. Due to this ~~region~~ reasion the reverse-biasing effect of drain is high then the reverse biasing effect of source. This explains why the deplation region penetrates further more into the channel ~~then~~ of drain then the source.

Now, ~~let~~, when gate-reverse voltage is disconnected then the cross-sectional area of channel is high which causes the max^m drain current $I_D = \frac{V_{DD}}{R_{DS}}$. Now, let V_{GG} is applied. As the gate bias, the deplation region (space charge) increases which causes the decrease in cross-section of drain due to which the drain current decreases. Since there are no charge carriers ~~available~~ available in deplation region, its conductivity

(6) When, we increase the gate reverse bias further more, then at a certain -ve gate-source voltage, the two depletion region near drain as shown in fig-2 touch each other and in this case drain current becomes zero. Thus, we see that for fixed value of V_{DD}, we can vary the drain current controlled by gate voltage. Due to this fact, the FET is called voltage controlled-current device.

FET characteristic

i) Drain characteristic (static characteristic)
ii) Transfer characteristic.

(7)

Static Drain characteristic of JFET

The curve drawn bet drain current I_D and drain to source voltage V_{DS} for different values of V_{GS} is called Drain characteristic. The fig-1. shows ckt arrangement for drawing drain characteristic.

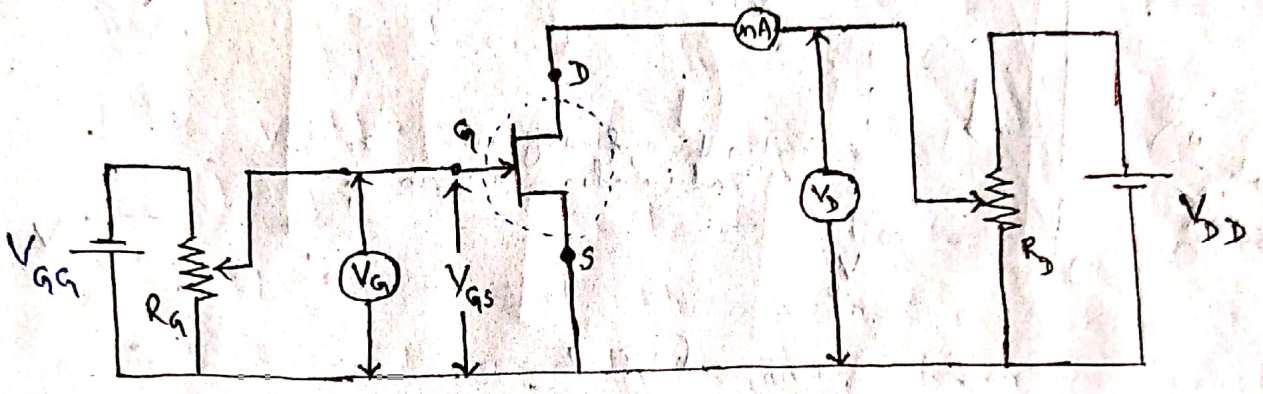


Fig-1.

Ckt consist of an N-channel FET, Potentio-meter R_D and R_G are used to vary V_{DS} and V_{GS}. The drain current I_D is measured by milli-ammeter (mA) connected in series with drain terminal and supply V_{DD}.

Working:- First of all, we set V_{GS} to zero and increase V_{DS} in small suitable steps and note down corresponding value of I_D in each steps. The similar process is repeated for different values of V_{GS} as $V_{GS} = +0.5V, -1V, -2V$ etc and note-down the corresponding values of I_D.

(8) When, we plot a graph for V_{DS} and I_D, we obtained a curve, as shown in fig-2 called, drain characteristic.

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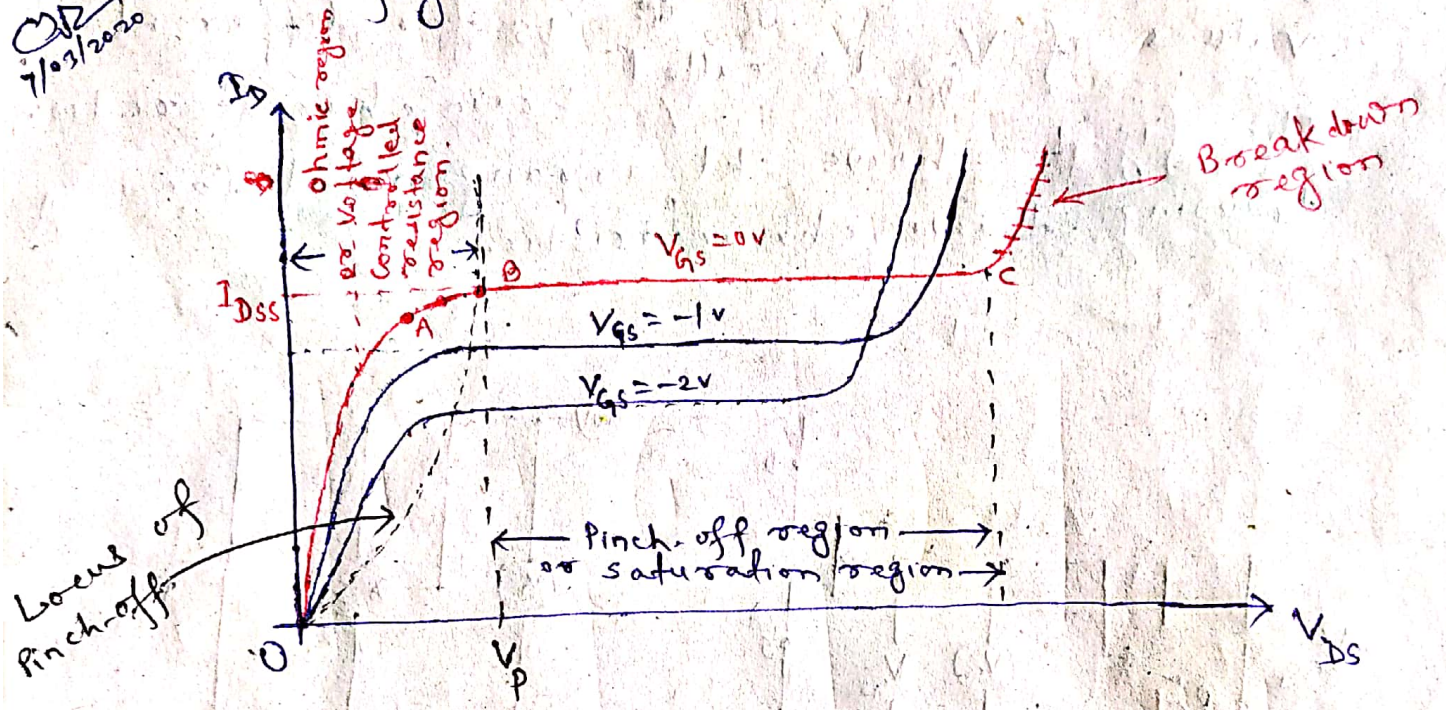


Fig-2

Analysis

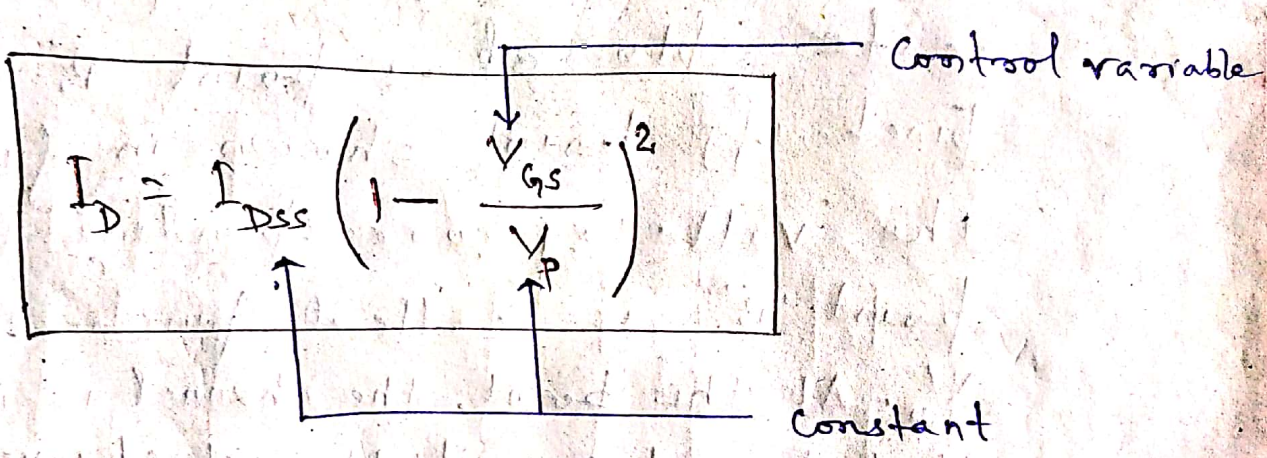
When, $V_{GS}=0$, $V_{DS}=0$, no attracting pot' at the drain and hence drain curren $I_D=0$. As V_{DS} is increased, the electroons flow from source to drain through channel between depletion layers and drain current I_D increases linearly upto a point 'A' (knee-point). 'OA' shows, in this region FET behaves like an ordinary resistor till point A.

Now, if we increase V_{DS} and correspondingly I_D, the ohmic-voltage drop in the material bar, reverse biases the gate junction and

consequently, the channel region begins to constrict. The constriction is unequal along the length, being more at distances farther from source. Thus, if V_{DS} progressively increase the drain current I_D, from point 'A' increases at reverse square-law rate upto a point 'B' called pinch-off point shown in fig-2. The voltage corresponding to this point 'B' is called pinch-off voltage V_p. At this point, the channel is more or less blocked and current through channel almost becomes constant I_{DSS} called saturation-drain current. Thus, the minimum drain-to-source voltage where drain current approaches a constant value (saturation value), is called pinch-off voltage. Beyond pinch-off voltage, the channel width can not be reduced. Here it should be remembered that, pinch-off does not mean drain current I_D cut-off moreover the channel is not completely closed.

As, V_{DS} is further increased, the channel resistance also increases in such a way that I_D practically remains constant upto a point 'C' shown in graph. The region 'BC' is called saturation-region or "amplifier-region".

In this region 'BC' FET operates as constant-current device (offering very large resistance, ideally infinity). A relationship bet^n I_D and V_{GS} is given by "William Broadford shockley" called shockley eq^n as below ——



With continued increase of V_{DS} corresponding to point C (called avalanche breakdown), eventually breakdown across the gate junction takes places and I_D shoots to a high value.

Miller Theorem

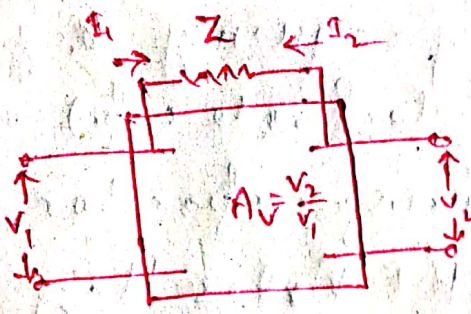


Fig- 1(a)

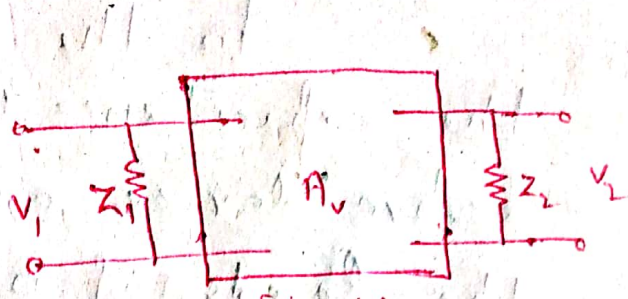


Fig- 1(b)

Miller theorem states that, if an impedance Z is connected between input and output terminal of a two port network with gain A_v, then this impedance can be replaced by connecting $Z_1 = \frac{Z}{1-A_v}$ into input side and $Z_2 = \frac{Z}{1-A_v^{-1}}$ into output side as shown in above fig.

Analysis.

$$I_1 = \frac{V_1 - V_2}{Z} = \frac{V_1\left(1 - \frac{V_2}{V_1}\right)}{Z} = \frac{V_1(1-A_v)}{Z}$$

$$\Rightarrow I_1 = \frac{V_1}{\left(\frac{Z}{1-A_v}\right)} = \frac{V_1}{Z_1}, \text{ where } Z_1 = \frac{Z}{1-A_v}$$

And,

$$I_2 = \frac{V_2 - V_1}{Z} = \frac{V_2\left(1 - \frac{V_1}{V_2}\right)}{Z} = \frac{V_2(1-A_v^{-1})}{Z}$$

$$\Rightarrow I_2 = \frac{V_2}{\left(\frac{Z}{1-A_v^{-1}}\right)} = \frac{V_2}{Z_2}, \text{ where } V_2 = \frac{Z}{1-A_v^{-1}}$$

07/03/2020

Miller Effect capacitance

In the high frequency region, the capacitance (inter-electrode cap.) of active device and wiring capacitor bet" the leads of network takes play a vital role. For inverting, the input and output capacitance is increased by capacitance level sensitive to the inter-electrode capacitance bet" I/p and o/p terminals of device and the gain of amplifier. i.e there is a feedback process. This feedback capacitance is C_f.

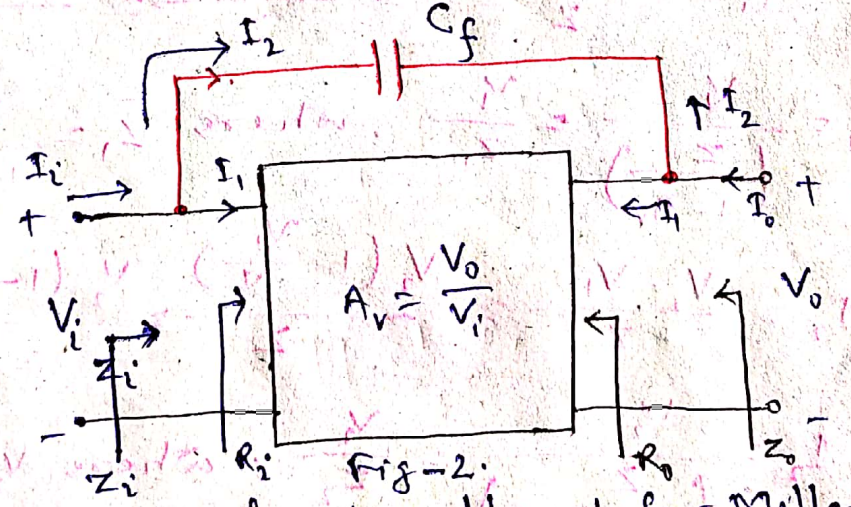


Fig-2.
(Network employed for Miller's cap.)

Apply KCL at input-port —

$$I_i = I_1 + I_2 \quad \text{——— (i)}$$

Now, $I_i = \frac{V_i}{Z_i}$ ——— (ii)

and, $I_1 = \frac{V_i}{R_i}$ ——— (iii)

$I_2 = \frac{V_i - V_o}{X_{cf}}$ ——— (iv)

From eq^n (i), (ii), (iii) & (iv)

$I_i = I_1 + I_2 \Rightarrow \frac{V_i}{Z_i} = \frac{V_i}{R_i} + \frac{V_i - V_o}{X_{cf}}$

since $A_v = \frac{V_o}{V_i} \Rightarrow V_o = A_v V_i$.

$\therefore \frac{V_i}{Z_i} = \frac{V_i}{R_i} + \frac{V_i - A_v V_i}{X_{cf}}$

or $\frac{V_i}{Z_i} = V_i \left[\frac{1}{R_i} + \frac{(1 - A_v)}{X_{cf}}\right]$

or $\frac{1}{Z_i} = \frac{1}{R_i} + \frac{1}{\left\{\frac{X_{cf}}{(1 - A_v)}\right\}}$

i.e $Z_i = R_i \| \left\{\frac{X_{cf}}{(1 - A_v)}\right\}$

which follows the statement of Miller's theorem. Hence $\left(\frac{X_{cf}}{1 - A_v}\right)$ is termed as Miller's capacitive reactance at input side.

Let $X_{CM_i} = \frac{X_{cf}}{1 - A_v}$.

then,

$$X_{C_{M_i}} = \frac{X_{C_f}}{1 - A_v}$$

or $$\frac{1}{j\omega C_{M_i}} = \frac{1}{j\omega C_f (1 - A_v)}$$

$$\Rightarrow \boxed{C_{M_i} = (1 - A_v) C_f}$$

In similar manner, in output side —

$$I_o = I_1 + I_2 \quad \text{or} \quad \frac{V_o}{Z_o} = \frac{V_o}{R_o} + \frac{V_o - V_i}{X_{C_f}}$$

$$\text{or} \quad \frac{V_o}{Z_o} = \frac{V_o}{R_o} + \frac{\left(V_o - \frac{V_o}{A_v}\right)}{X_{C_f}}$$

$$\text{or} \quad \frac{1}{Z_o} = \frac{1}{R_o} + \frac{\left(1 - \frac{1}{A_v}\right)}{X_{C_f}} \quad \Rightarrow \frac{1}{Z_o} = \frac{1}{R_o} + \frac{1}{\frac{X_{C_f}}{(1 - 1/A_v)}}$$

$$\text{or} \quad Z_o = R_o \| \left(\frac{X_{C_f}}{1 - 1/A_v}\right)$$

Let, $X_{C_{M_o}} = \frac{X_{C_f}}{1 - 1/A_v}$ or $\frac{1}{j\omega C_{M_o}} = \frac{1}{j\omega C_f (1 - 1/A_v)}$

$$\Rightarrow \boxed{C_{M_o} = \left(1 - \frac{1}{A_v}\right) C_f}$$

If $A_v \gg 1$, then, $C_{M_o} \approx C_f$.

2. DISTORTION

For an ideal amplifier, the output corresponding to sinusoidal input should be sinusoidal. But practically, output is not just the replica of input. The change in output waveform in comparision to input signal waveform is known as distortion. There are following types of distortions —

i) Nonlinear distortion (OR Amplitude distortion)
ii) Frequency distortion
iii) phase-shift distortion.

i) Nonlinear distortion :- The distortion which results due to the production of new frequency components in output which was not present in input, is called 'non-linear distortion. This distortion is caused mainly due to non-linear behaviour of active element.

ii) Frequency distortion :- The distortion which come into existence when different frequency components are amplified differently. In BJT or F.E.T, such type of distortion come into existance due to internal capacitance or associated ckt (Coupling components or load) is due reactive.

iii) Phase shift distortion :- This type of distortion come int existance when different freq. component shifte at different or from unequal phase angle. Phase shift is funct^n of freq.