Programmable Peripheral Interface

INTEL-8255

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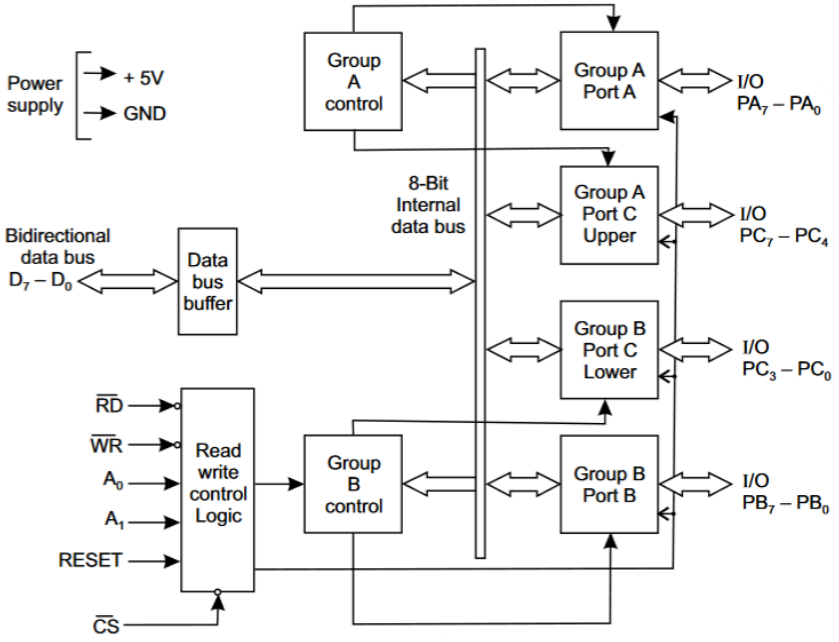
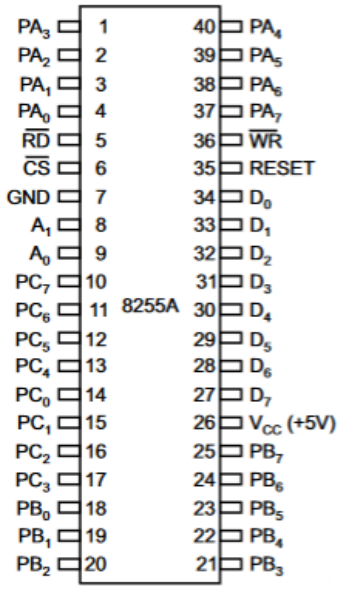
The 8255 is a general purpose programmable, Parallel I/O device designed for use with Intel microprocessors. It consists of three 8-bit bidirectional I/O ports (24 I/O lines) that can be programmed to transfer data under various conditions from simple I/O to interrupt I/O.

The three ports are PORT A, PORT B & PORT C. Port A contains one 8-bit output latch/buffer and one 8-bit input buffer. Port B is same as PORT A. However, PORT C can be split into two parts PORT C lower (PC0-PC3) and PORT C upper (PC7-PC4) by the control word. The three ports are divided in two groups Group A (PORT A and upper PORT C) Group B (PORT B and lower PORT C).

Block Diagram:



Pin Diagram:



Read write control logic:

The function of this block is to manage all the internal and external transfers of both data and control or status word. The details of each pin connected with this block are described below.

$\overline{CS}$ (Chip Select)- A "Low" on this input pin enables the communication between the 8085 and MPU.

A_0 and A_1- These are the address lines of 8255 which are directly connected to the MPU lower address lines (A_0, A_1). The bit combination of these signals are shown below.

$\overline{cs}$	A_1	A_0	Selection
0	0	0	Port A
0	0	1	Port B
0	1	0	Port C
0	1	1	Control Word Register
1	X	X	8255 is not selected

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PPI 8255 can operate in three modes:

(a) Mode 0 (b) Mode 1 and (c) Mode 2.

Apart from these there is another mode called BSR mode (Bit Set/Reset mode)

The three modes are Mode 0, Mode 1 and Mode 2. These are I/O operations and selected only if D7 bit of the control word register is put as 1. The three operating modes of 8255 are distinguished in the following manner:

Mode 0: This is a basic or simple input/output mode, whose features are:

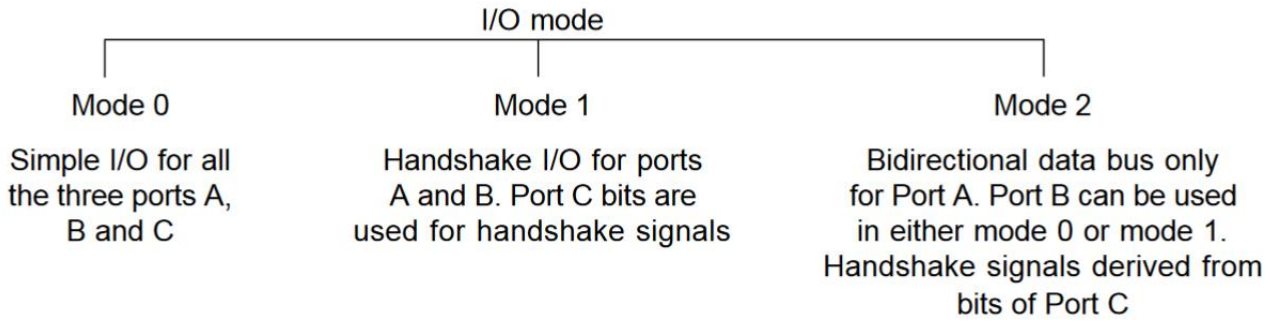
- Outputs are latched.
- Inputs are not latched.
- All ports (A, B, C_U, C_L) can be programmed in either input or output mode.
- Ports don't have handshake or interrupt capability.
- Sixteen possible input/output configurations are possible.

Mode 1: In this mode, input or outputting of data is carried out by taking the help of handshaking signals, also known as strobe signals. The basic features of this mode are:

- Ports A and B can function as 8-bit I/O ports, taking the help of pins of Port C.
- I/Ps and O/Ps are latched.
- Interrupt logic is supported.
- Handshake signals are exchanged between CPU and peripheral prior to data transfer.
- In this mode, Port C is called status port.
- There are two groups in this mode—group A and group B. They can be configured separately. Each group consists of an 8-bit port and a 4-bit port. This 4-bit port is used for handshaking in each group.

Mode 2: In this mode, Port A can be set up for bidirectional data transfer using handshake signals from Port C. Port B can be set up either in mode 0 or mode 1.

The basic operations of the three modes are shown below:



The control word format, when 8255 is operated in I/O mode, is shown below. For 8255 PPI to be operated in I/O mode, D7 bit must be 1.

The three ports are divided into two groups—Groups A and B. Group A consists of Port A and C_U (PC_4–PC_7) . Port A can be operated in any of the modes—0, 1 or 2. Group B consists of Port B and C_L(PC_0–PC_3). Here Port B can be operated in either mode 0 or 1.

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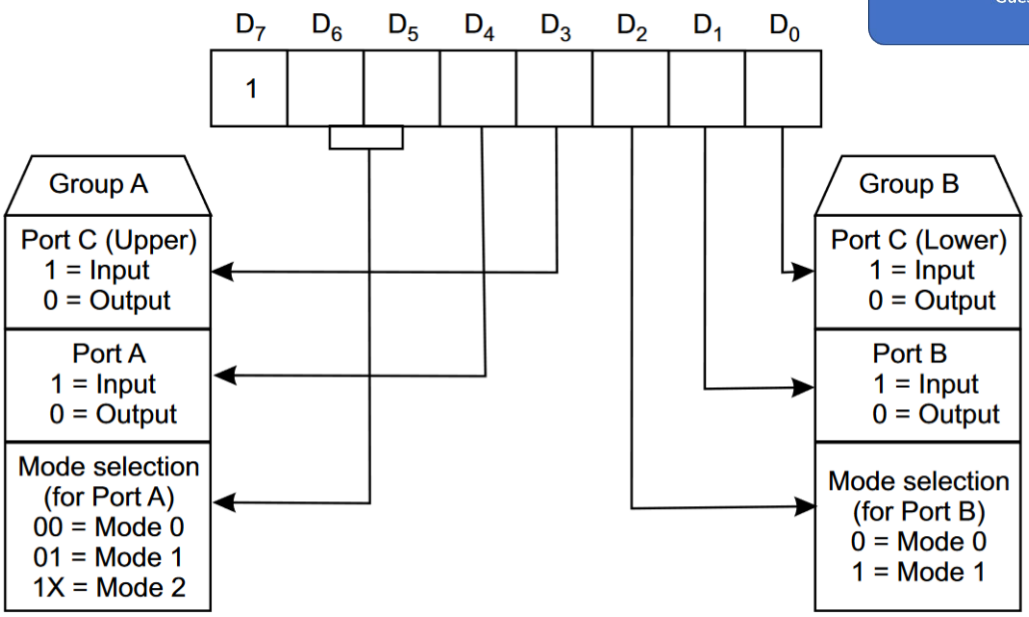


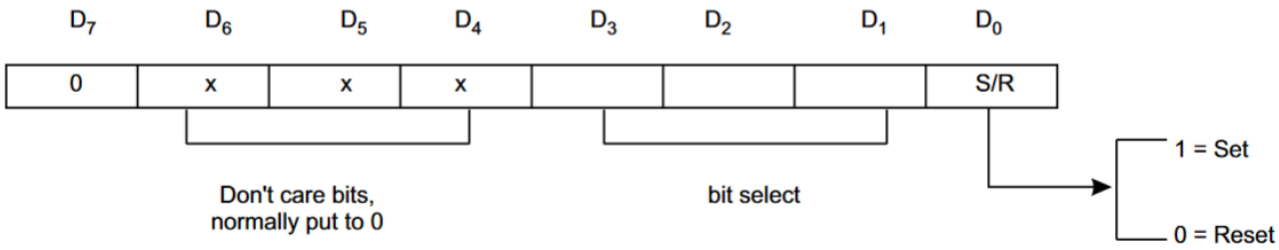
Fig: The CWR in the I/O mode

BSR (Bit Set Reset mode):

BSR mode stands for Bit Set Reset mode. The characteristics of BSR mode are:

- BSR mode is selected only when D_7 = 0 of the Control Word Register (CWR).
- It is concerned with bits of port C.
- Individual bits of Port C can either be Set or Reset.
- At a time, only a single bit of port C can be Set or Reset.
- Is used for control or on/off switch.
- BSR control word doesn't affect ports A and B functioning.

The content of the control word register will be as follows, when used in the BSR mode and selects (either Sets or Resets) a particular bit of Port C at a time



D_3	D_2	D_1	*Particular bit of Port C selected*
0	0	0	Bit 0
0	0	1	Bit 1
0	1	0	Bit 2
0	1	1	Bit 3
1	0	0	Bit 4
1	0	1	Bit 5
1	1	0	Bit 6
1	1	1	Bit 7

Fig: The CWR in the BSR mode