# EXPERIMENT NO: 10

**AIM:** TO DESIGN &VERIFY OPERATION OF HALF ADDER &FULL ADDER.

**APPARATUS REQUIRED:** Power supply, IC's , Digital Trainer, Connecting leads .

**BRIEF THEORY:** We are familiar with ALU, which performs all arithmetic and logic operation but ALU doesn't perform/ process decimal no's. They process binary no's.

**Half Adder:** It is a logic circuit that adds two bits. It produces the O/P, sum & carry.The Boolean equation for sum & carry are

$$SUM = A + B$$
$$CARRY = A.\ B$$

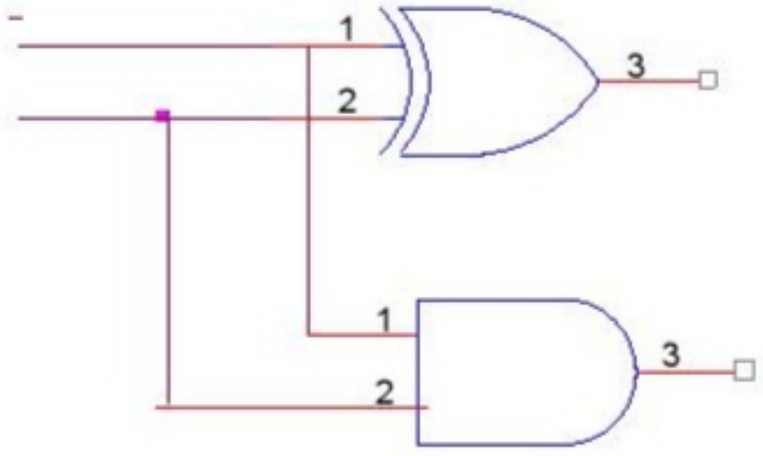
Therefore, sum produces 1 when A&B are different and carry is 1when A&B are 1. Application of Half adder is limited.

**Full Adder:** It is a logic circuit that can add three bits. It produces two O/P sum & carry. The Boolean Equation for sum & carry are

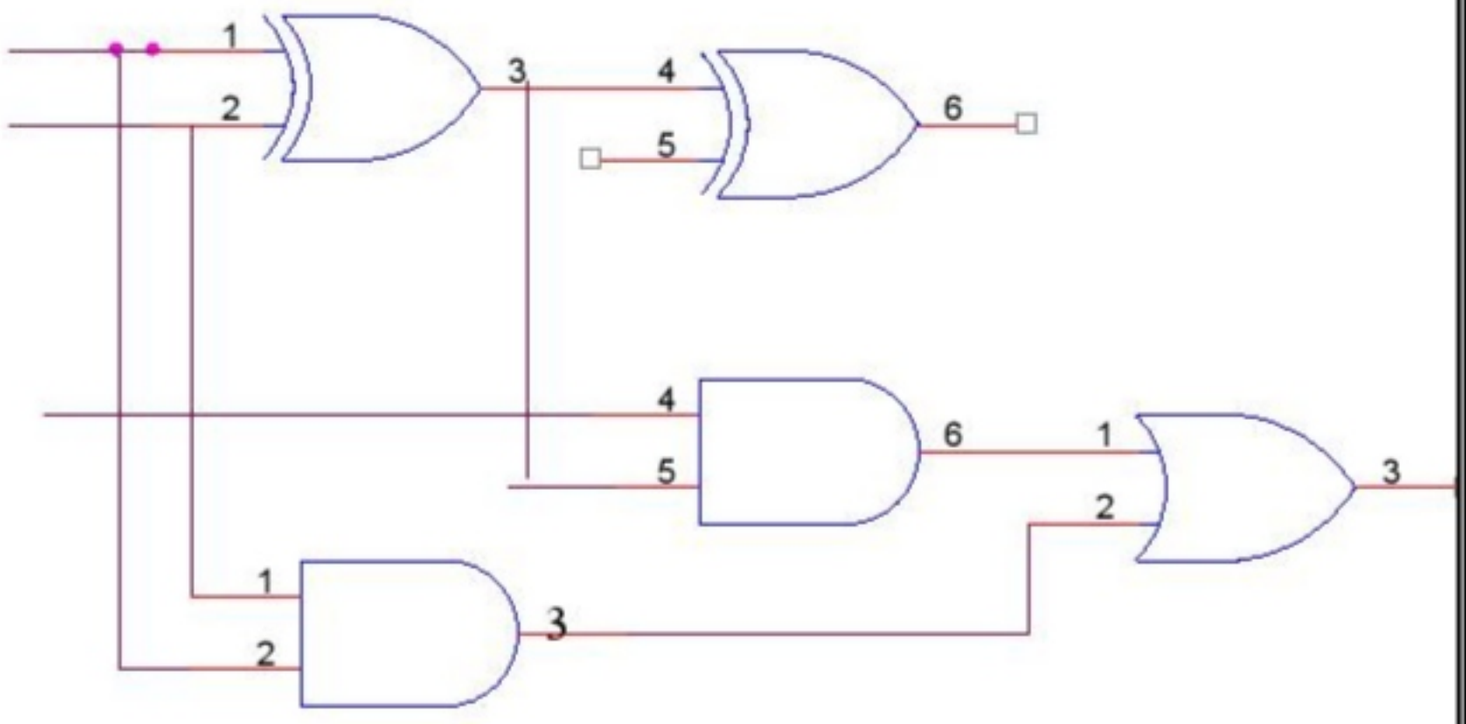
$$SUM = A + B + C$$
$$CARRY = A.B + (A+B)\ C$$

Therefore, sum produces one when I/P is containing odd no's of one & carry is one when there are two or more one in I/P.

**CIRCUIT DAIGRAM**




HALF ADDER




FULL ADDER

**PROCEDURE:**

(a) Connect the ckt. as shown in fig. For half adder.
(b) Apply diff. Combination of inputs to the I/P terminal.
(c) Note O/P for Half adder.
(d) Repeat procedure for Full wave.
(e) The result should be in accordance with truth table.

**OBSERVATION TABLE:**

**HALF ADDER:**

| INPUTS | | OUTPUT | |
|---|---|---|---|
| A | B | S | C |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

**FULL ADDER:**

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| A | B | C | S | CARRY |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

**RESULT:** The Half Adder & Full Adder ckts. are verified.

**PRECAUTIONS:**

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.