**AIM:** VERIFICATION OF STATE TABLES OF RS, JK, T AND D FLIP-FLOPS USING NAND & NOR GATES

**APPARATUS REQUIRED:** IC' S 7400, 7402 Digital Trainer & Connecting leads.

**BRIEF THEORY:**

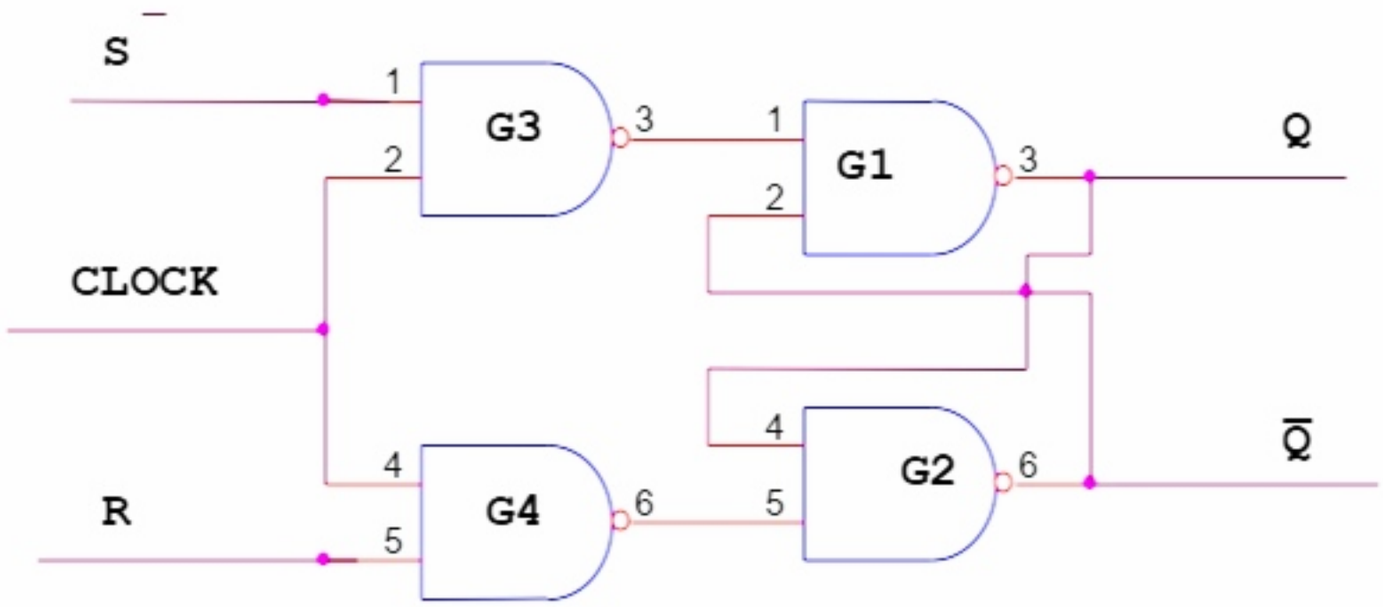
- **RS FLIP-FLOP:** There are two inputs to the flip-flop defined as R and S. When I/Ps R = 0 and S = 0 then O/P remains unchanged. When I/Ps R = 0 and S = 1 the flip-flop is switches to the stable state where O/P is 1 i.e. SET. The I/P condition is R = 1 and S = 0 the flip-flop is switched to the stable state where O/P is 0 i.e. RESET. The I/P condition is R = 1 and S = 1 the flip-flop is switched to the stable state where O/P is forbidden.

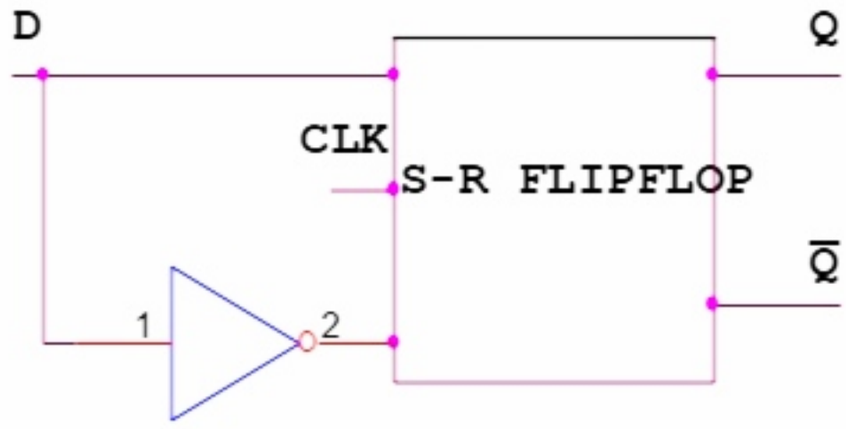
- **JK FLIP-FLOP**: For purpose of counting, the JK flip-flop is the ideal element to use. The variable J and K are called control I/Ps because they determine what the flip- flop does when a positive edge arrives. When J and K are both 0s, both AND gates are disabled and Q retains its last value.

- **D FLIP –FLOP**: This kind of flip flop prevents the value of D from reaching the Q output until a clock pulse occur. When the clock is low, both AND gates are disabled D can change value without affecting the value of Q. On the other hand, when the clock is high, both AND gates are enabled. In this case, Q is forced to equal the value of D. When the clock again goes low, Q retains or stores the last value of D. a D flip flop is a bistable circuit whose D input is transferred to the output after a clock pulse is received.

- **T FLIP-FLOP**: The T or "toggle" flip-flop changes its output on each clock edge, giving an output which is half the frequency of the signal to the T input. It is useful for constructing binary counters, frequency dividers, and general binary addition devices. It can be made from a J-K flip-flop by tying both of its inputs high.

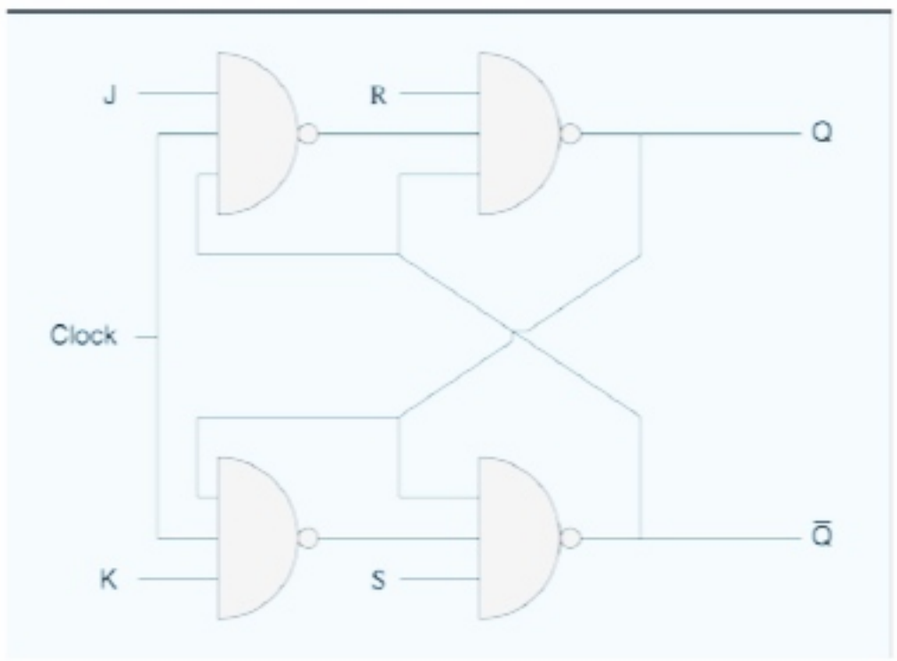
## CIRCUIT DIAGRAM:

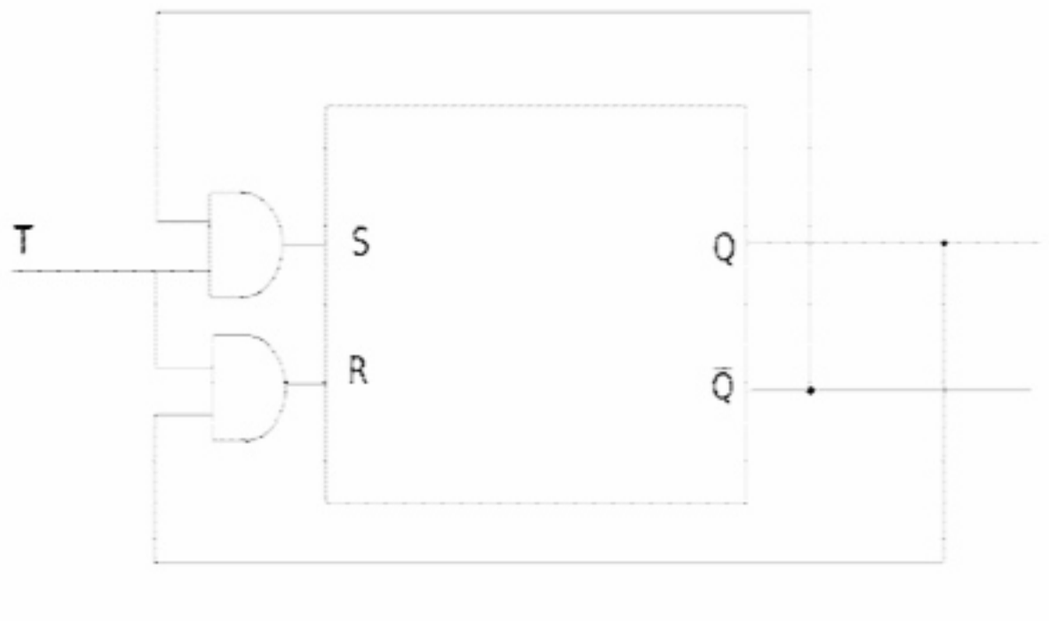



SR FLIPFLOP

D FLIPFLOP




JK FLIPFLOP

T FLIPFLOP

## PROCEDURE:

1. Connect the circuit as shown in figure.
2. Apply Vcc & ground signal to every IC.
3. Observe the input & output according to the truth table.

## OBSERVATION TABLE:

### SR FLIP FLOP:

| CLOCK | S | R | $Q_{n+1}$ |
|---|---|---|---|
| 1 | 0 | 0 | NO CHANGE |

| | | | |
|---|---|---|---|
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | ? |

## D FLIPFLOP:

| INPUT | OUTPUT |
|---|---|
| 0 | 0 |
| 1 | 1 |

## JK FLIPFLOP

| CLOCK | S | R | $Q_{n+1}$ |
|---|---|---|---|
| 1 | 0 | 0 | NO CHANGE |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | Qn’ |

## T FLIPFLOP

| CLOCK | S | R | $Q_{n+1}$ |
|---|---|---|---|
| 1 | 0 | 1 | NO CHANGE |
| 1 | 1 | 0 | Qn’ |

**RESULT:** Truth table is verified on digital trainer.

**PRECAUTIONS**:

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The $V_{cc}$ and ground should be applied carefully at the specified pin only.