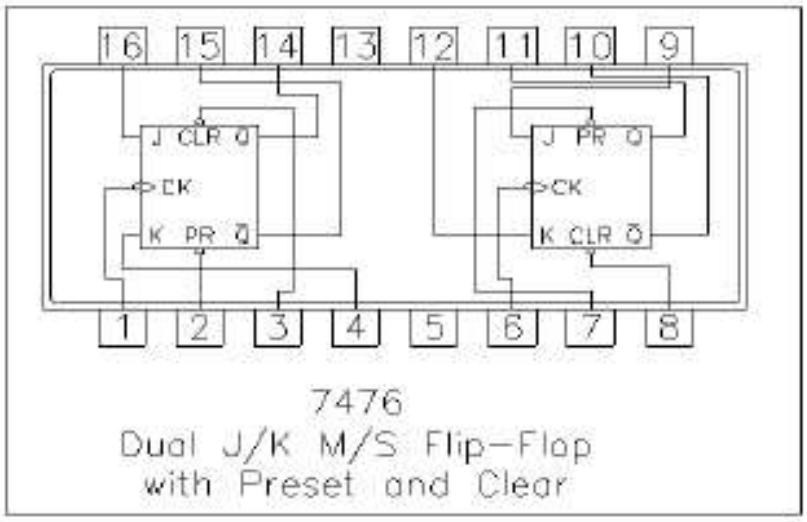
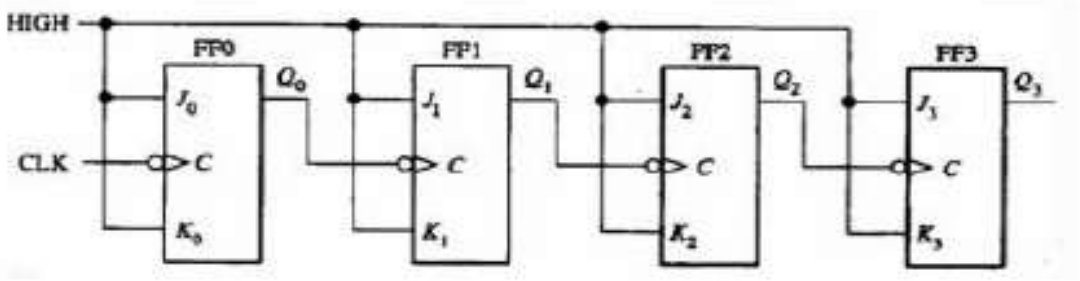
AIM – DESIGN, AND VERIFY THE 4-BIT ASYNCHRONOUS COUNTER

APPARATUS REQUIRED – Digital trainer kit and 4 JK flip flop each IC 7476 (i.e dual JK flip flop) and two AND gates IC 7408.

BRIEF THEORY: Counter is a circuit which cycle through state sequence. Two types of counter, Synchronous counter (e.g. parallel) and Asynchronous counter (e.g. ripple). In Ripple counter same flip-flop output to be used as clock signal source for other flip-flop.Synchronous counter use the same clock signal for all flip-flop

PIN CONFIGURATION;–





CIRCUIT DIAGRAM

Pin Number	Description
1	Clock 1 Input
2	Preset 1 Input
3	Clear 1 Input
4	J1 Input
5	Vcc
6	Clock 2 Input
7	Preset 2 Input
8	Clear 2 Input
9	J2 Input
10	Complement Q2 Output
11	Q2 Output
12	K2 Input
13	Ground
14	Complement Q1 Output
15	Q1 Output
16	K1 Input

PROCEDURE –

a)Make the connections as per the logic diagram
b)Connect +5v and ground according to pin configuration
c)Apply diff combinations of inputs to the i/p terminals.
d)Note o/p for summation
e)Verify the truth table.

RESULT- 4-bit asynchronous counter studied and verified.

PRECAUTIONS:

4. Make the connections according to the IC pin diagram.
5. The connections should be tight.
6. The V_{cc} and ground should be applied carefully at the specified pin only.