Name of Experiment:- Characterization of Digital Logic Families.

Introduction

Objectives

This experiment includes characterization of TTL NAND gate and CMOS gate

- How to characterize different logic families
- How to analyze logic operations of different logic families

Theory

TTL NAND Gate:

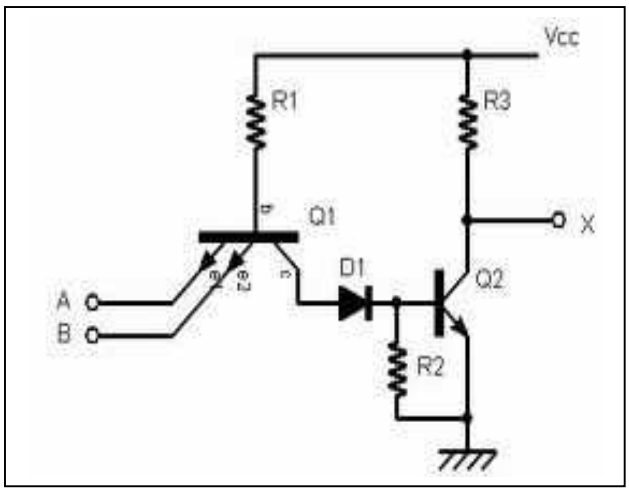


Figure: 01 Multiple Input Emitter Structure of TTL

In the above diagram if any input is low, the corresponding base-emitter junction becomes forward-biased and the transistor conducts.

Logical Operation

A table of conduction states has been drawn up showing the state of each transistor in the circuit for all possible input conditions to verify the logic function performed. The direction of conduction of T1 can be in the forward or reverse mode so this should also be noted in the table. It can be seen from the table that the output goes LOW only when both inputs are HIGH which verifies the NAND function.

Vi1	Vi2	T1	T2	T3	T4	D	V0
LOW	LOW	ON(for)	OFF	OFF	ON	ON	HIGH
LOW	HIGH	ON(for)	OFF	OFF	ON	ON	HIGH
HIGH	LOW	ON(for)	OFF	OFF	ON	ON	HIGH
HIGH	HIGH	ON(rev)	OFF	OFF	ON	ON	LOW

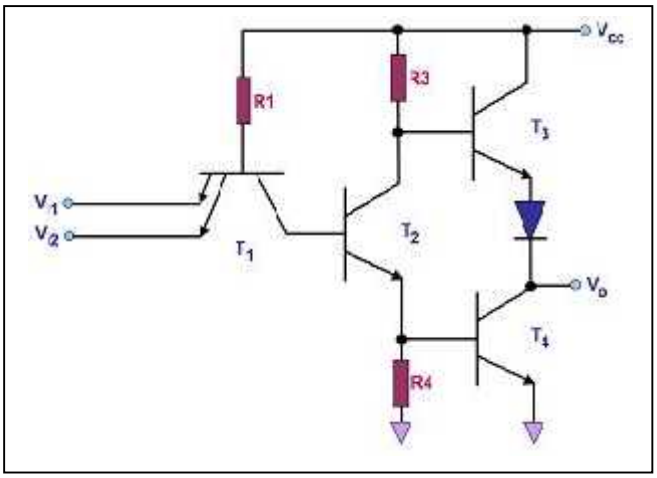


Figure 2: Circuit Diagram of a Standard 2-input TTL NAND Gate

CMOS NAND Gate:

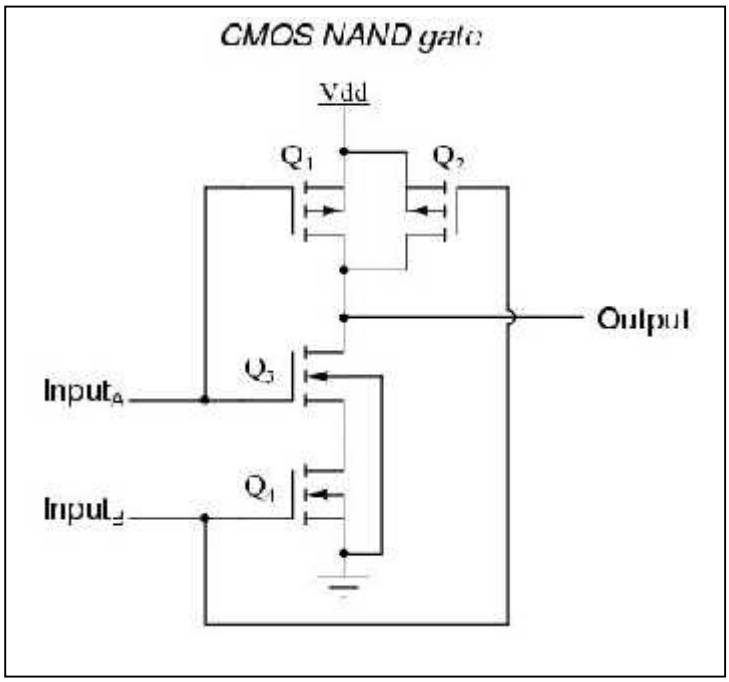


Fig 3: Q1,Q2: PMOS Q3,Q4: NMOS

More complex logic functions such as those involving AND and OR gates require manipulating the paths between gates to represent the logic. When a path consists of two transistors in series, both transistors must have low resistance to the corresponding supply voltage, modeling an AND. When a path consists of two transistors in parallel, either one or both of the transistors must have low resistance to connect the supply voltage to the output, modeling an OR. Shown on the right is a circuit diagram of a NAND gate in CMOS logic. If both of the A and B inputs are high, then both the NMOS transistors (bottom half of the diagram) will conduct, neither of the PMOS transistors (top half) will conduct, and a conductive path will be established between the output and Vss (ground), bringing the output low.

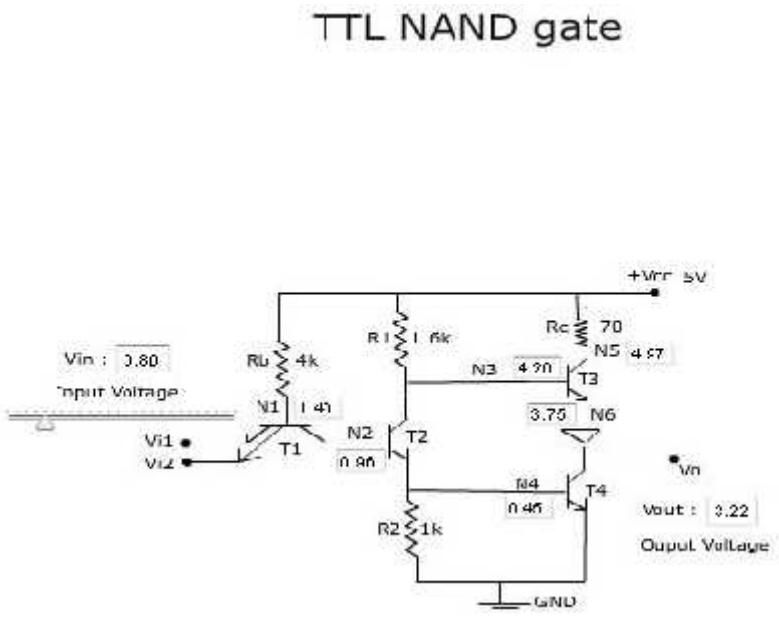
If either of the A or B inputs is low, one of the NMOS transistors will not conduct, one of the PMOS transistors will, and a conductive path will be established between the output and Vdd (voltage source), bringing the output high.

Procedure

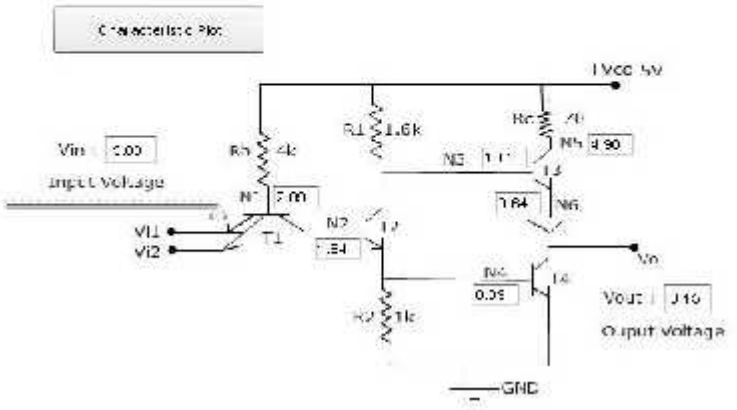
Follow these steps to do the experiment.

Part 1: .TTL NAND gate circuit

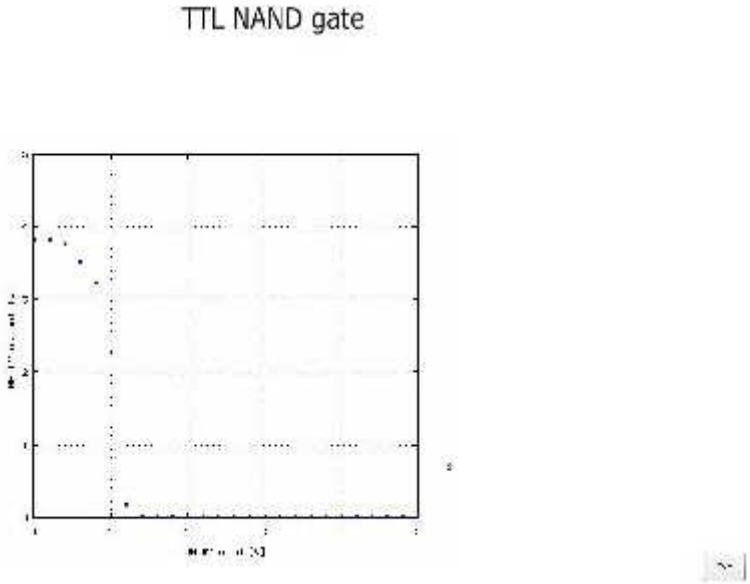
1. At first change the input voltage. Then observe the corresponding voltage at each node and also obseve the output voltage.



2. At the time of changing the input voltage, when input voltage reaches 5 voltage characteristic plot button will be appeared.

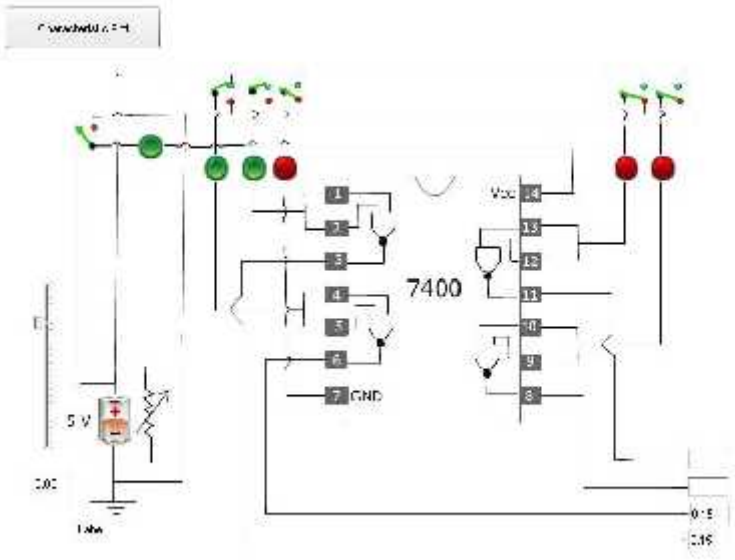


3. Next, Click on the characteristic plot. Characteristic plot will be appeared.
4. Next, Click on the exit button.

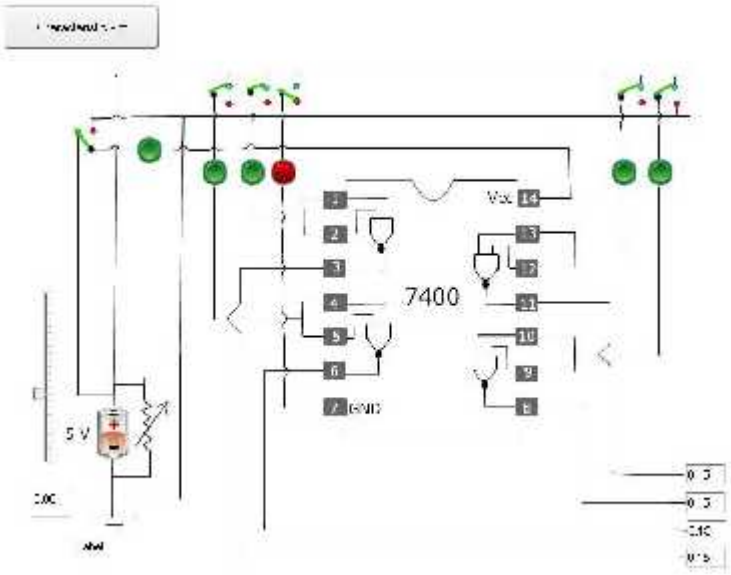


Part 2: TTL NAND gate using IC 7400

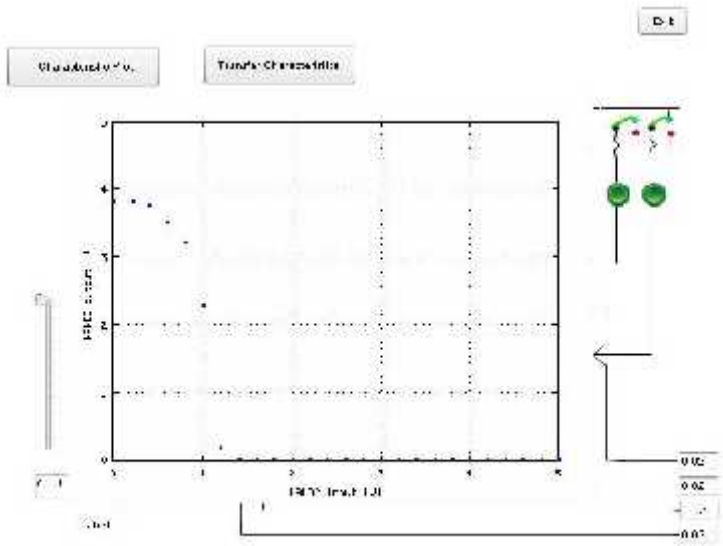
1. At first connect VCC and GND properly. Apply high voltage to VCC and apply low voltage to GND.
2. Next, apply high voltage to one of the NAND gate inputs among four.
3. Next, Change the input voltage level. Then observe the corresponding output voltage of that particular NAND gate.



4. If we apply high voltage to each NAND gate input we get coresponding output voltage of each NAND gate.

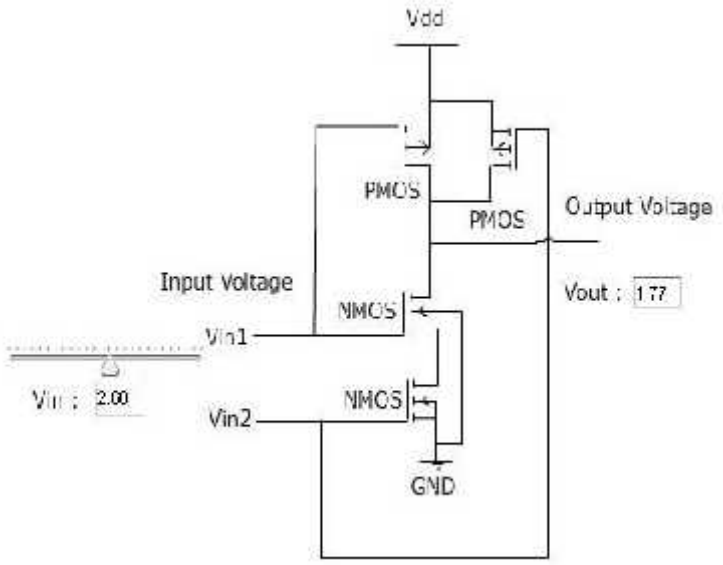


5. Click on characteristic plot. Then corresponding plot will be appeared.

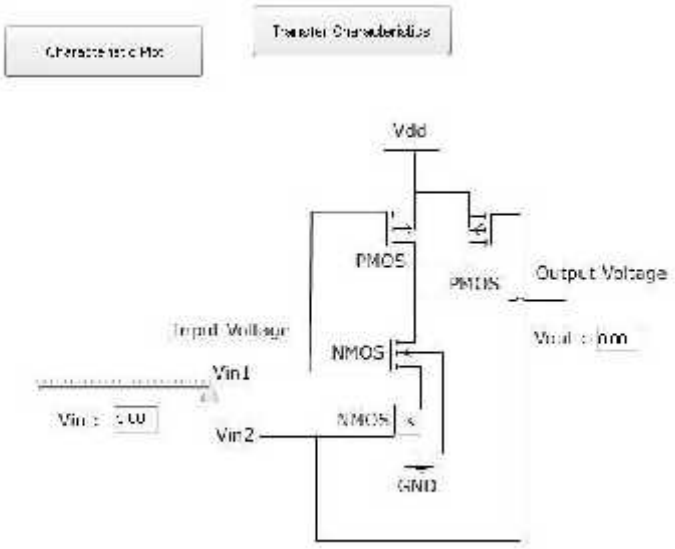


Part 3: CMOS NAND gate circuit

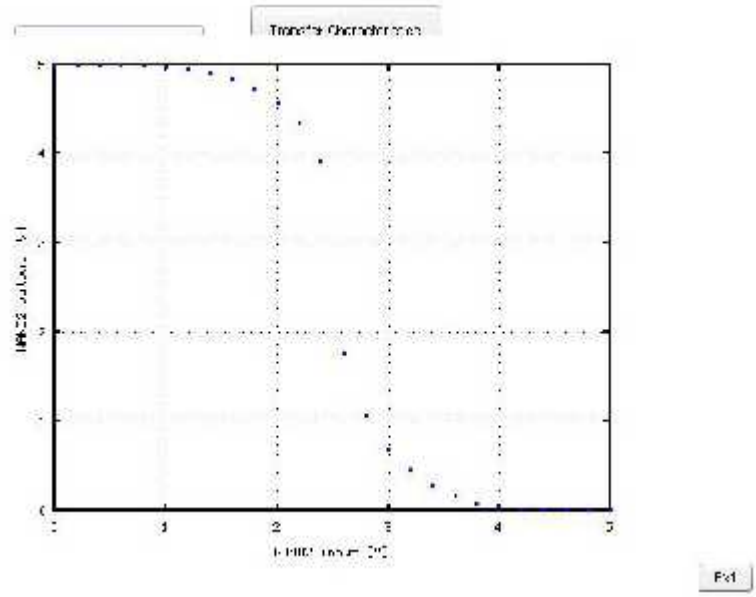
1. When we change the input voltage the corresponding output voltage will be appeared.



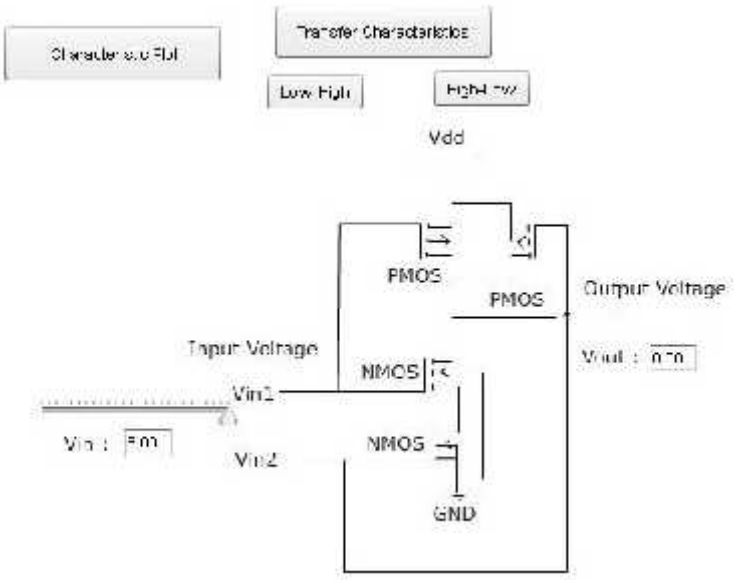
2. At the time of changing the input voltage, when it reaches 5 voltage characteristic plot and transfer-characteristic buttons will be appeared.



3. Next, Click on the characteristic plot. Characteristic plot will be appeared.
4. Next, Click on the exit button.



5. Next, Click on the Transfer characteristic button. High to Low and Low to High options will be appeared.



6. Next, click on the High to Low option.The plot will be appeared.
7. Next, click on the Low to High option.The plot will be appeared.

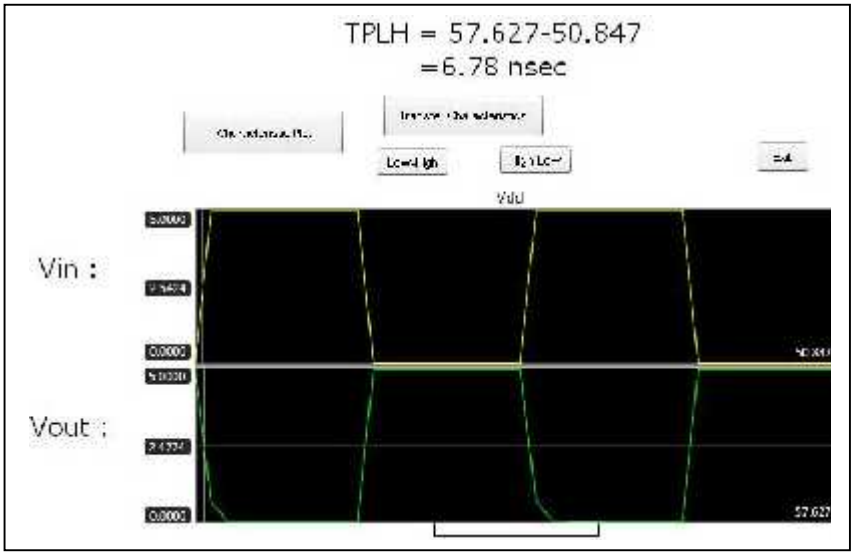


Fig: a) High to Low

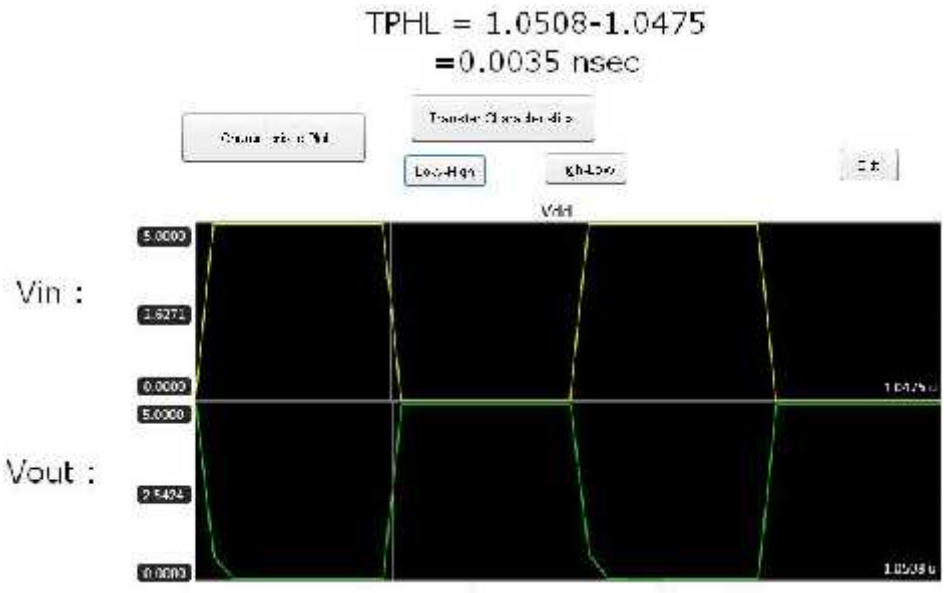
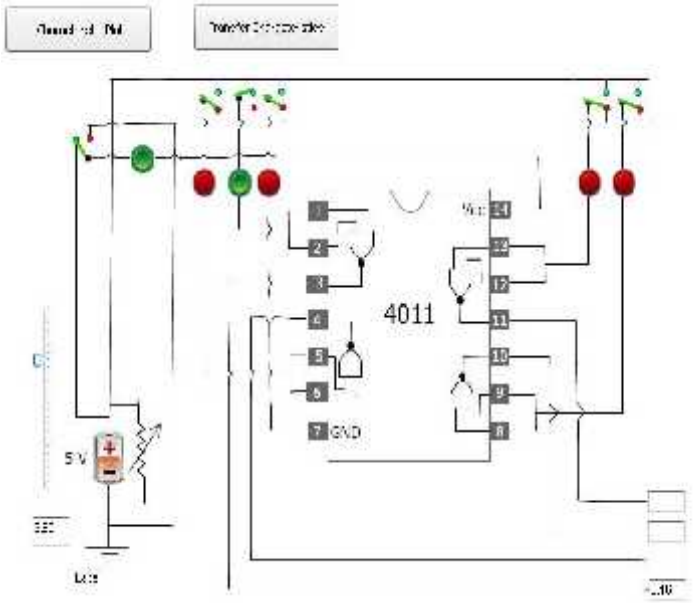


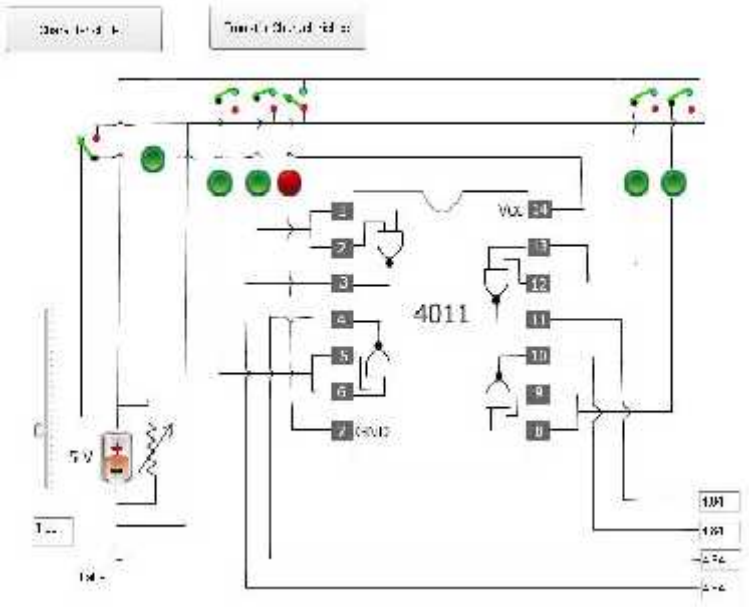
Fig: b) Low to High

Part 4: CMOS NAND gate using IC 4011

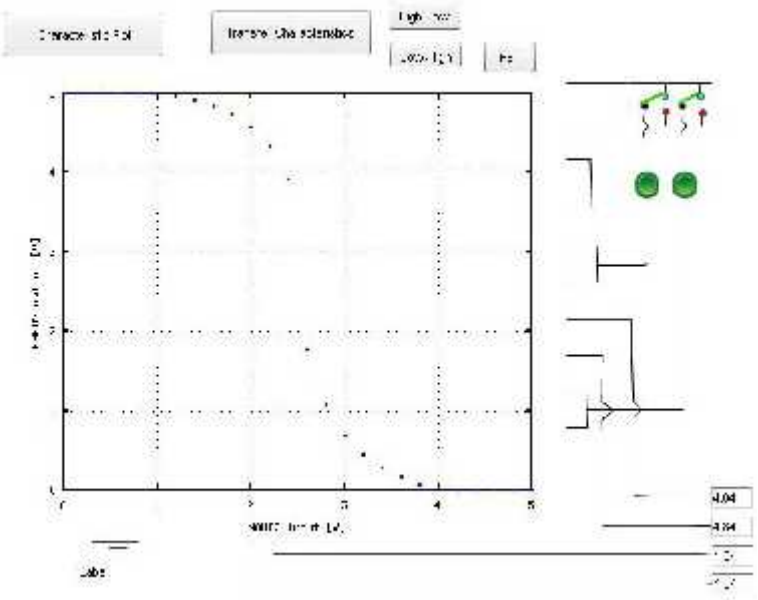
1. At first connect VCC and GND properly. Apply high voltage to VCC and apply low voltage to GND.
2. Next, apply high voltage to one of the NAND gate inputs among four.
3. Change the input voltage level. Then observe the corresponding output voltage of that particular NAND gate.



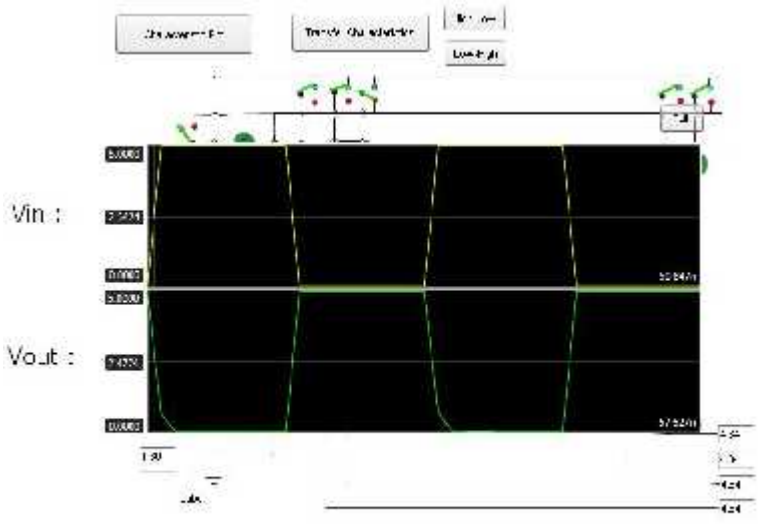
4.If we apply high voltage to each NAND gate input we get corresponding output voltage of each NAND gate.



5. Click on characteristic plot. Then corresponding plot will be appeared.



6. After clicking Transfer characteristic button two options, such as High to Low and Low to High will be appeared.
7. Next click on High to Low and Low to High respectively. Corresponding plot will be appeared. Then click on Exit button to go back to the experiment.



TPLH = 57.627-50.847

Fig: a) High to Low

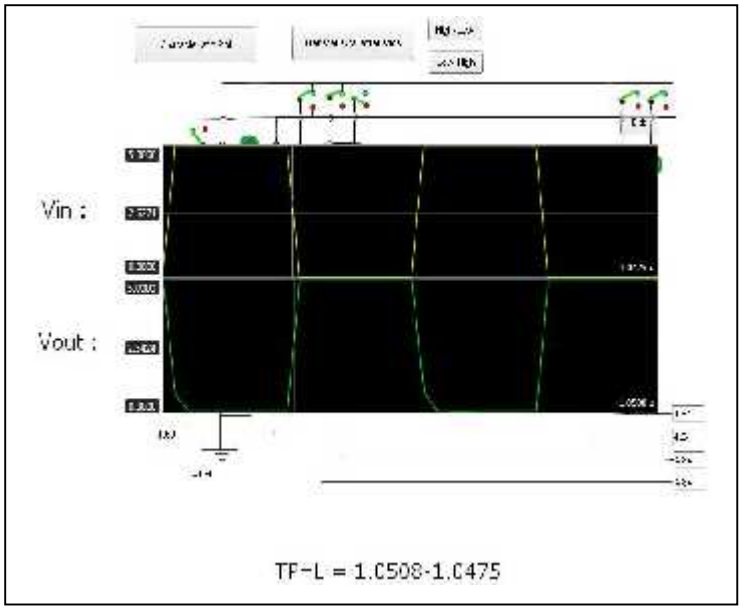


Fig: b) Low to High