13.9.7 Analog-to-Digital Converter using Voltage-to-Time Conversion

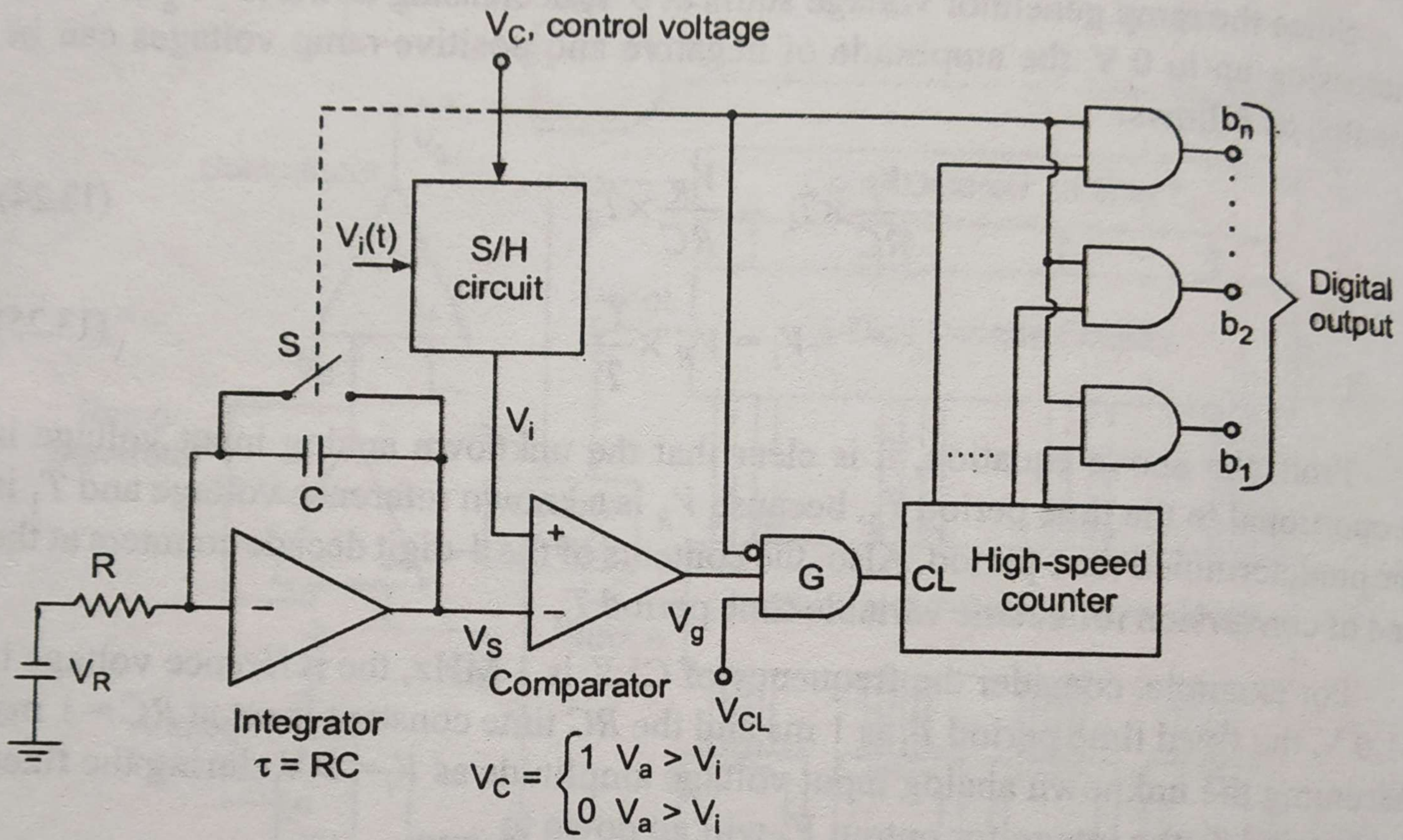
An analog signal can be converted into digital signal by counting the pulses from a variable frequency source whose frequency is dependent on the analog input signal value. The counting is done for a fixed period of time. Alternatively, the pulses from a fixed frequency source can be counted for a variable period of time, and the time period is then dependent on the analog signal under conversion.

Fig. 13.27 (a) shows such an A/D converter. It employs an integrator, a Sample-and-Hold (S/H) circuit, a voltage comparator and a high-speed counter. A negative reference voltage V_R is applied to the integrator, which integrates the voltage V_R and provides a positive polarity output. The analog signal input under conversion $V_i(t)$ is sampled at a rate fixed by the control voltage V_c, and the sampled signal at any instant

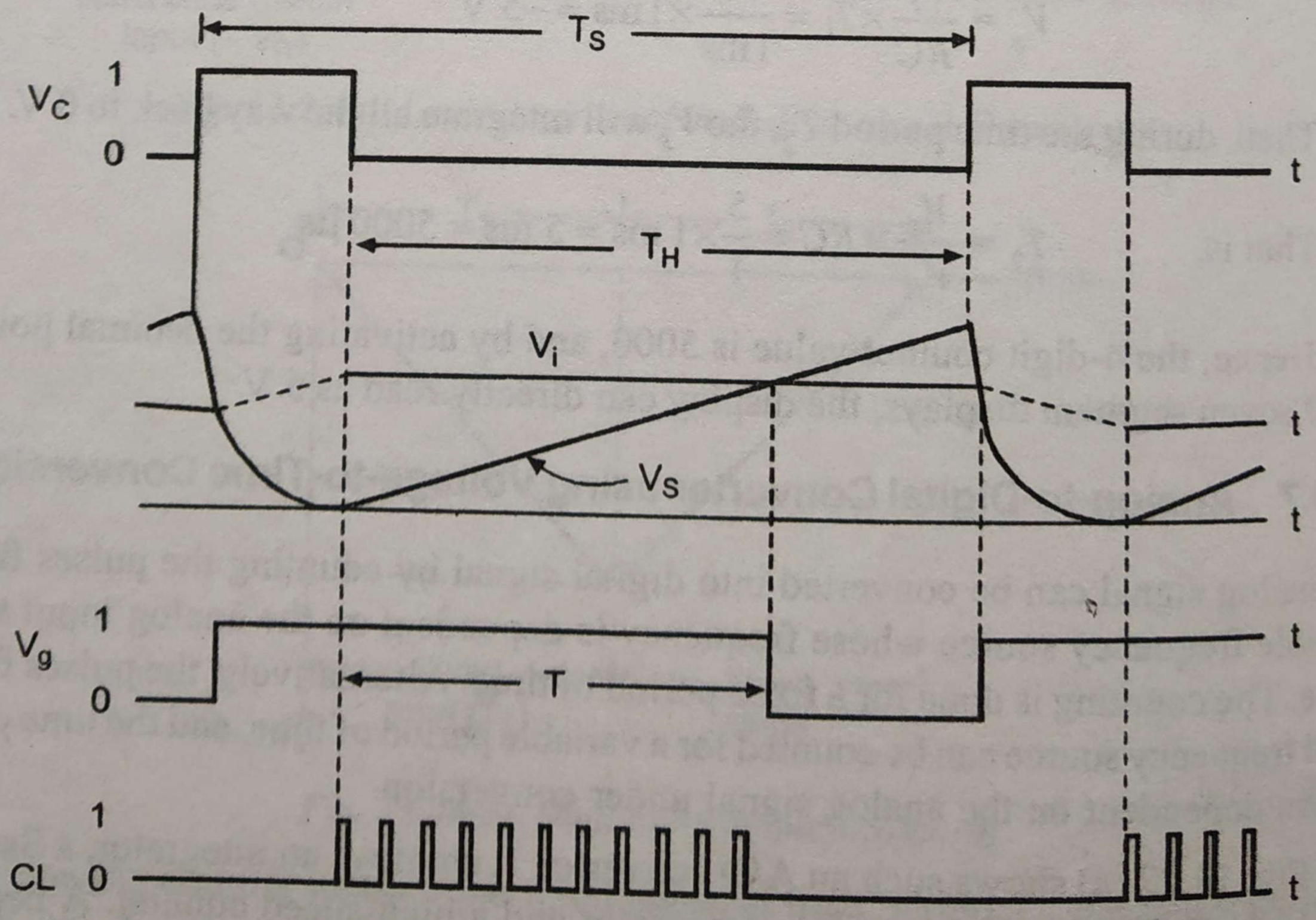
V_i is applied as input to the noninverting terminal of comparator. The integrator output V_s is connected to the inverting input of comparator.

When the integrated voltage V_s is less than the analog voltage sample V_i as shown in Fig. 13.27(b), the comparator output is at *positive* saturation, or a logic 1.

A fixed frequency clock V_{CL} is applied to the high-speed counter through the AND gate G. The AND gate is enabled for the duration from $t = 0$ when $V_i = 0$ to the time $t = T$ when $V_s = V_i$.



(a)



(b)

***Fig. 13.27** An A/D converter using a voltage-to-time converter (a) Functional block diagram; (b) Input and output waveforms*

We know that $V_s = \frac{V_R t}{\tau}$ where the time constant is given by $\tau = RC$ for the integrator.

Therefore, at time $t = T$ when $V_s = V_i$, we can infer

$$T = \frac{\tau V_i}{V_R} \tag{13.26}$$

Assuming F_C is the clock frequency, the count output N obtained during the time interval 0 to T is given by

$$N = F_C T = \frac{\tau F_C V_i}{V_R} \tag{13.27}$$

Hence, the count value N is proportional to V_i.

Figure 13.27(b) shows the waveforms of the sampling control voltage V_c, output of comparator V_g and the clock output CL. The operation of the circuit can be analyzed as follows.

The Sample-and-Hold circuit samples the positive input voltage $V_i(t)$ for every T_A. Then the sampled voltage V_i is held for a time duration indicated by T_H in Fig. 13.27(b). During the period T_H, the switch S is held *open*, and the integrator operates with its output following a ramp voltage waveform V_s. When $V_s < V_i$, the comparator output V_g is at logic 1, and the gate G is enabled, with V_c in 0 state. This continues for a time interval T and during this time, the clock pulses are passed by the gate G to the high-speed counter. Thus the digital output of the counter is directly proportional to T. During the time interval T_A, the gate is disabled, and the digital output is read from the counter. The switch S is closed during T_A, and the capacitor discharges, resetting V_s to 0 V thus starting a new conversion.

13.9.2 Counter Type A/D Converter

The counter type A/D converter is constructed using only one comparator with a variable reference voltage. The variable reference voltage can be obtained by a sequence or binary counter and a D/A converter. The block diagram for an *n*-bit counter type A/D converter is shown in Fig. 13.19 (a).

The operation of the counter type A/D converter is as follows. The *n*-bit binary counter is initially set to 0 by the *Reset* switch which is normally active LOW. Therefore, the digital output is zero and the analog equivalent V_r is also 0. When Reset signal is released (HIGH), the clock pulses gated through the AND gate are counted by the binary counter. The D/A converter converts the digital output to an analog voltage and connects it as the inverting input to the comparator. The output of the comparator enables the AND gate to pass the clock. The number of counted pulses increases with time and the analog output V_r from DAC is a rising staircase waveform as shown in Fig. 13.19(b).

The counting will continue until the reference voltage V_r equals and just rises more than V_i. Then the comparator output becomes LOW and this disables the AND gate from passing the clock. The counting stops at the instance $V_i < V_r$ and at that instant the digital output of the comparator represents the analog input voltage V_i. Then the clock is inhibited, the counter stops its progress and the conversion is said to be complete. The numbers stored in the *n*-bit counter is the equivalent *n*-bit digital data for the given analog input voltage.

In this A/D converter, the counter advances by one count for every clock pulse, and therefore, the clock speed decides the conversion speed. For example, if a 100 kHz clock is used in an 8-bit A/D converter, the counter advances for every step and it will take 2.56 ms (i.e., $2^8 \times \frac{1}{100\ \text{kHz}} = 2.56$ ms) to reach the full-scale digital output (i.e., $2^8 \times 10\ \mu s = 256$ ms). Normally, the time required to reach one half of the full-scale voltage is called *average conversion* time. Hence, the average conversion time of the above A/D converter is 1.28 ms.

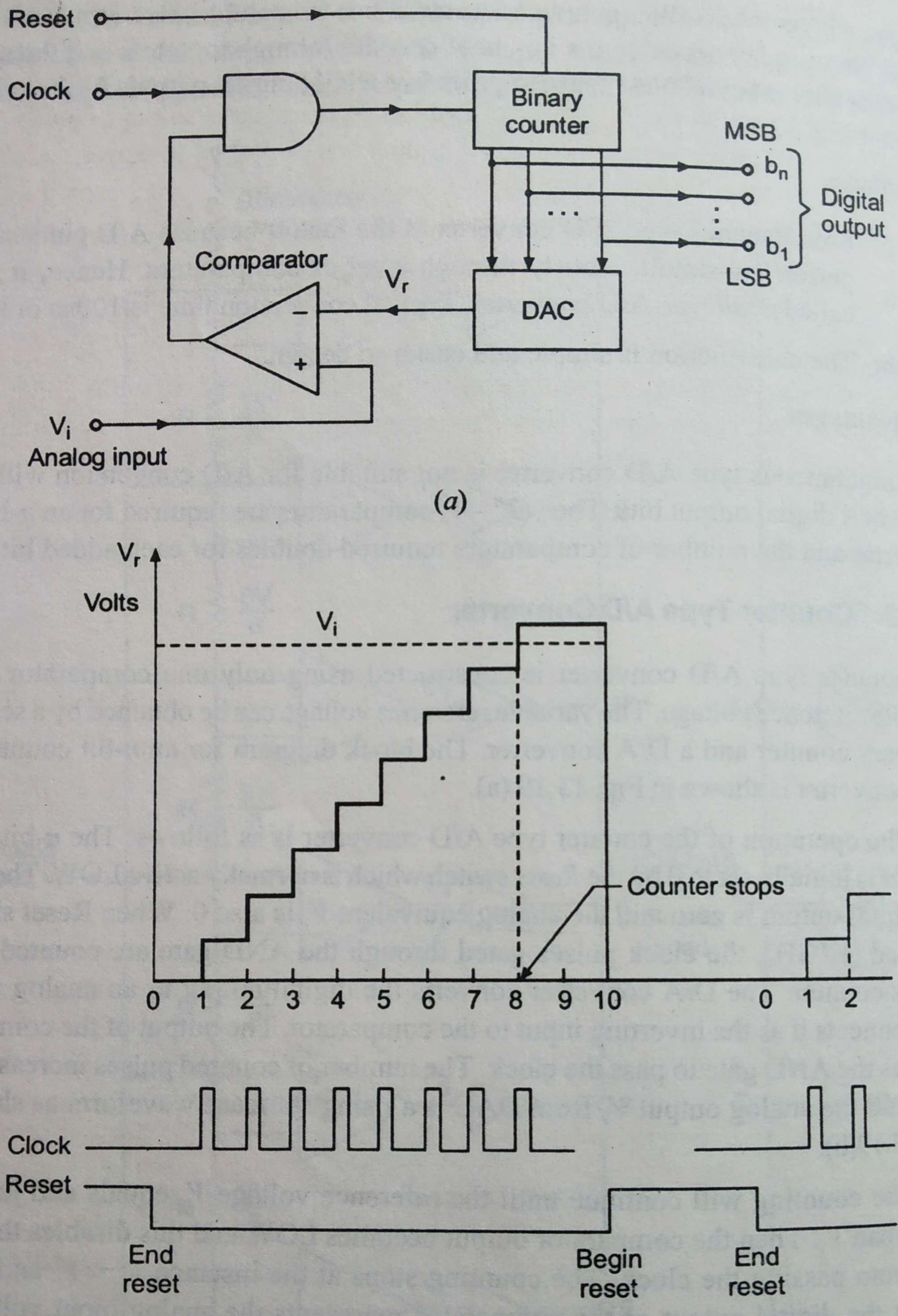


Fig. 13.19 Counter type A/D converter
(a) Block diagram; (b) Its output staircase waveform

Advantages

(i) The counter type A/D converter is very simple and needs less hardware compared to the simultaneous type A/D converter.

(ii) This is suitable for digitizing applications with high resolution.

Disadvantages

In counter type A/D converter, the conversion time is very long, variable and proportional to the amplitude of the analog input voltage. Since the counter always counts from 0 through a normal sequence, a maximum of 2^n counts are required to convert a full-scale analog input voltage. Hence, for an n-bit A/D converter, the average conversion time is $2^n/2 = 2^{n-1}$ times the clock period, which can be very long for large value of n.

13.9.6 Dual Slope Type A/D Converter

In dual slope type A/D converter, the integrator generates two different ramps, one with the unknown analog input voltage V_i as the input, and another with a known reference voltage $-V_R$ as the input. Hence, it is called *dual slope* type A/D converter. Its logic diagram is shown in Fig. 13.26(a) and the dual ramp output waveform in Fig. 13.26(b).

The operation of dual slope type A/D converter is explained as follows. Assume that the 4-digit decade counter is initially reset to 0000, the ramp output V_S is reset to 0 V, analog input voltage is positive, and the input to the ramp generator or integrator is switched to the unknown analog input voltage. Since the positive analog input voltage is connected to the inverting input of the integrator, the integrator output V_S is a negative ramp while the comparator output V_g is positive, and the CLK is passed through the AND gate. This results in counting-up of the 4-digit decade counter. The negative ramp will proceed for a fixed time period T_1, which is determined by a count

detector for the time period T_1. At the end of fixed time period T_1, the ramp voltage is given by

$$V_S = \frac{V_i}{RC} \times T_1 \tag{13.22}$$

where RC is the time constant of the ramp generator circuit.

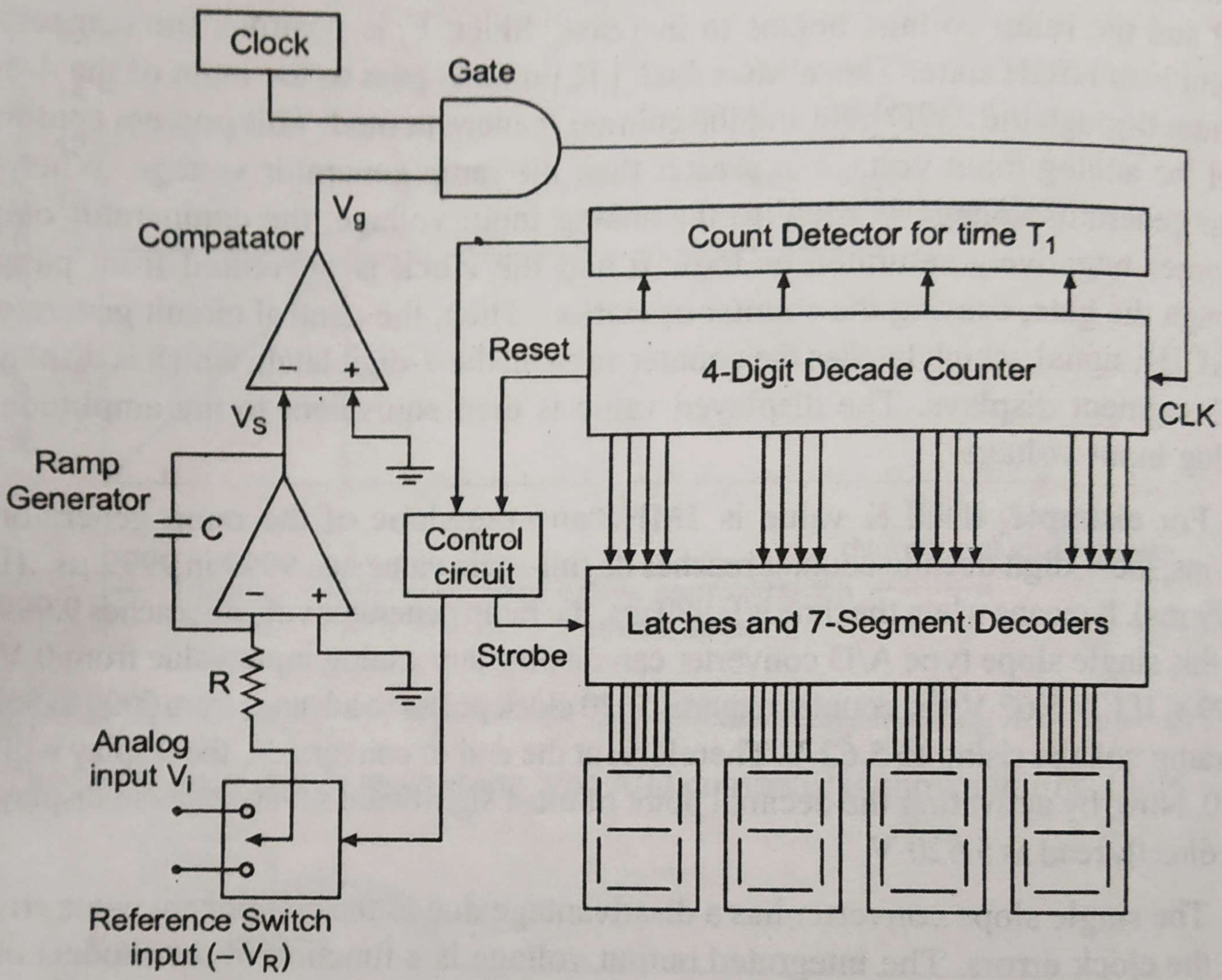


Fig. 13.26(a) Logic diagram of dual slope type A/D converter

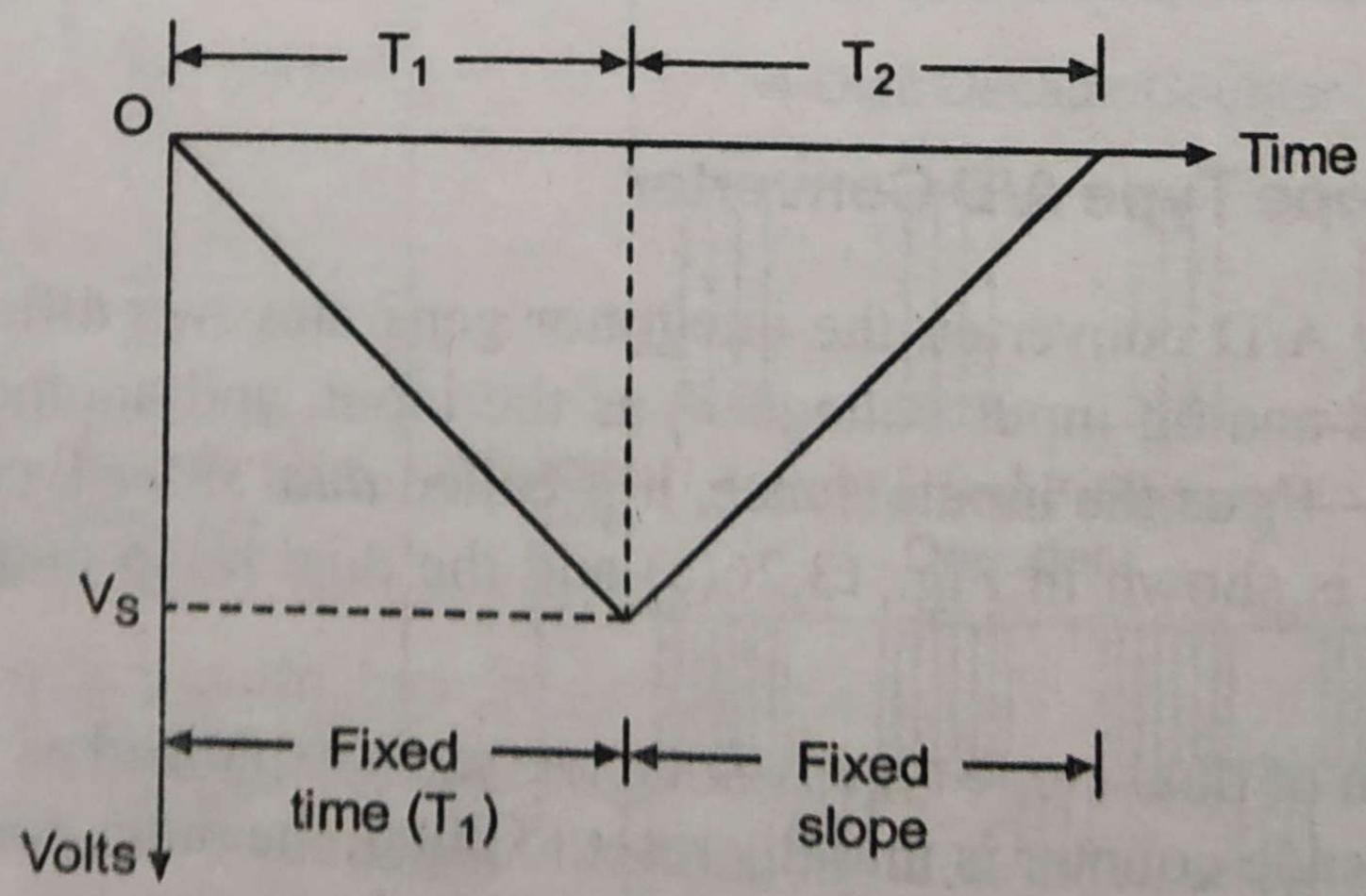


Fig. 13.26(b) Dual ramp output waveform

When the counter reaches the fixed count at time period T_1, the count detector gives a signal to the control circuit which in turn resets the counter to 0 and switches the integrator input to a negative reference voltage ($-V_R$). Now, the ramp generator begins at $-V_S$ and increases upward until it reaches 0 V. During this time, the counter

gets advanced. When V_S reaches 0 V, the comparator output will become 0 and the CLK is inhibited from passing through the AND gate. Now, the conversion cycle is said to be completed and the positive ramp voltage is given by

$$V_S = -\left(\frac{-V_R}{RC} \times T_2\right) \tag{13.23}$$

where V_R and RC are constants and the time period T_2 is variable.

Since the ramp generator voltage starts at 0 V, decreasing down to $-V_S$ and then increasing up to 0 V, the amplitude of negative and positive ramp voltages can be equated as follows:

$$-\frac{V_i}{RC} \times T_1 = \frac{V_R}{RC} \times T_2 \tag{13.24}$$

$$-V_i = V_R \times \frac{T_2}{T_1} \tag{13.25}$$

From the above equation, it is clear that the unknown analog input voltage is proportional to the time period T_2, because V_R is a known reference voltage and T_1 is the predetermined time period. Also, the contents of the 4-digit decade counters at the end of conversion reflect the variable time period T_2.

For example, consider the frequency of CLK is 1 MHz, the reference voltage is −1.0 V, the fixed time period T_1 is 1 ms and the RC time constant is set at $RC = 1$ ms. Assuming the unknown analog input voltage amplitude as $V_i = 5$ V, during the fixed time period T_1 the integrator output V_S will go down to

$$V_s = \frac{V_i}{RC} \times T_1 = \frac{-5}{1\,\text{ms}} \times 1\,\text{ms} = -5\ \text{V}$$

Then, during the time period T_2, the V_s will integrate all the way back to 0 V.

That is, $$T_2 = \frac{V_s}{V_R} \times RC = \frac{5}{1} \times 1\ \text{ms} = 5\ \text{ms} = 5000\ \mu\text{s}$$

Hence, the 4-digit counter value is 5000, and by activating the decimal point of MSD seven segment displays, the display can directly read as 5 V.

13.9.4 Successive Approximation Type A/D Converter

The conversion time is maintained constant in successive approximation type A/D converter, and it is proportional to the number of bits in the digital output, unlike the counter and continuous type A/D converters.

The basic principle of this A/D converter is that the unknown analog input voltage is approximated against an n-bit digital value by trying one bit at a time, beginning with the MSB. The principle of successive approximation process for a 4-bit conversion is shown in Fig. 13.21.

This type of A/D converter operates by successively dividing the voltage range by half, as explained in the following steps.

(i) The MSB is initially set to 1 with the remaining three bits set as 0. The digital equivalent is compared with the unknown analog input voltage.

(ii) If the analog input voltage is higher than the digital equivalent, the MSB is retained as 1 and the second MSB is set to 1. Otherwise, the MSB is reset to 0 and the second MSB is set to 1.

(iii) Comparison is made as given in step 1 to decide whether to retain or reset the second MSB. The third MSB is set to 1 and the operation is repeated down to LSB and by this time, the converted digital value is available in the SAR.

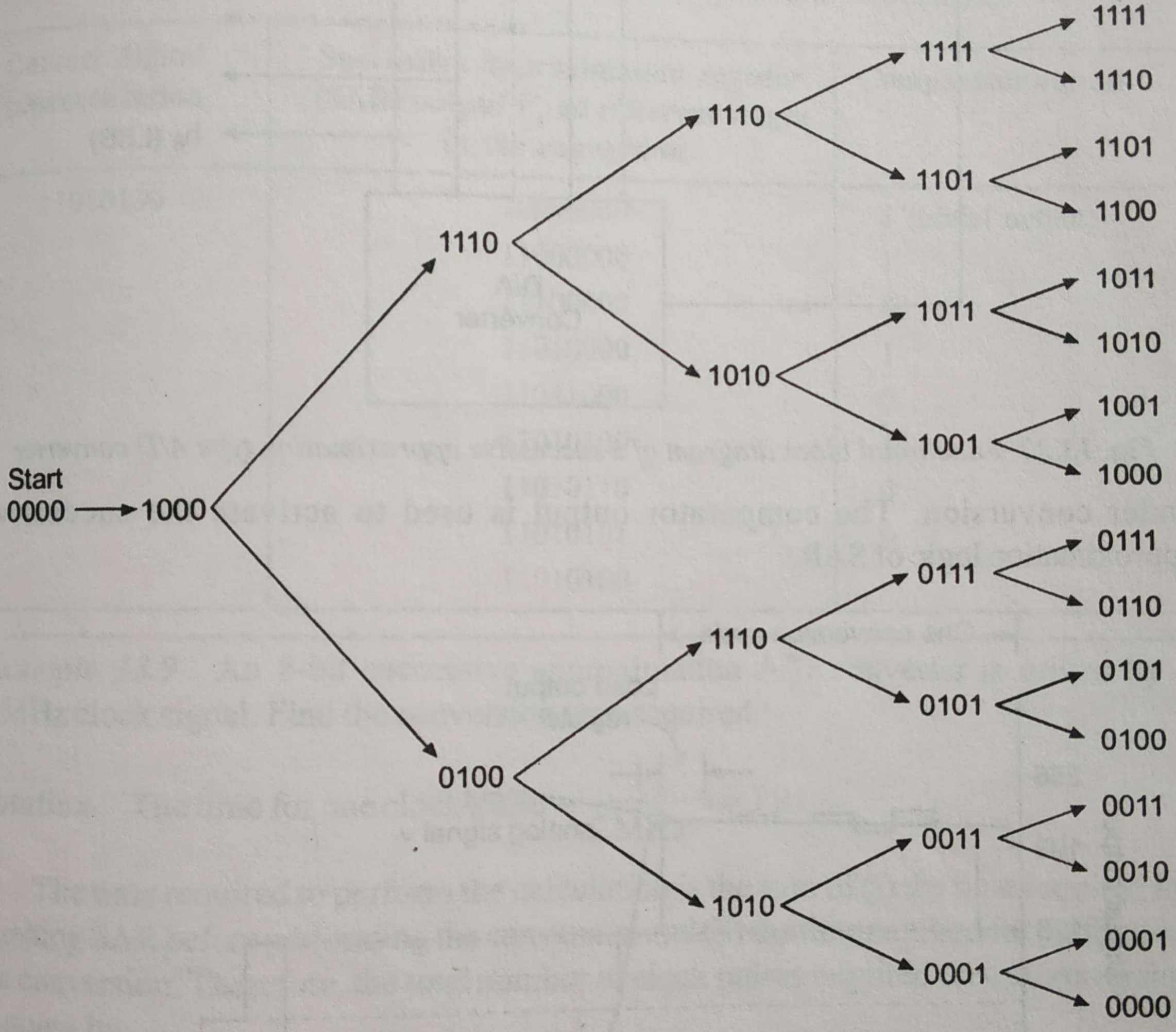


Fig. 13.21 Successive approximation principle for 4-bit digital output

From Fig. 13.21, it can be seen that the conversion time is constant (i.e., four cycles for 4-bit A/D converter) for various digital outputs. This method uses a very efficient search strategy to complete an *n*-bit conversion in just *n*-clock periods. Therefore, for an 8-bit successive approximation type A/D converter, the conversion requires only 8 cycles, irrespective of the amplitude of analog input voltage.

The functional block diagram of successive approximation type A/D converter is shown in Fig. 13.22. The circuit employs a *successive approximation register* (SAR) which finds the required value of each successive bit by *trial and error* method. The output of the SAR is fed to an *n*-bit D/A converter. The analog output equivalent of the D/A converter is applied to the noninverting input of the comparator, while the other input of the comparator is connected with the unknown analog input voltage V_i

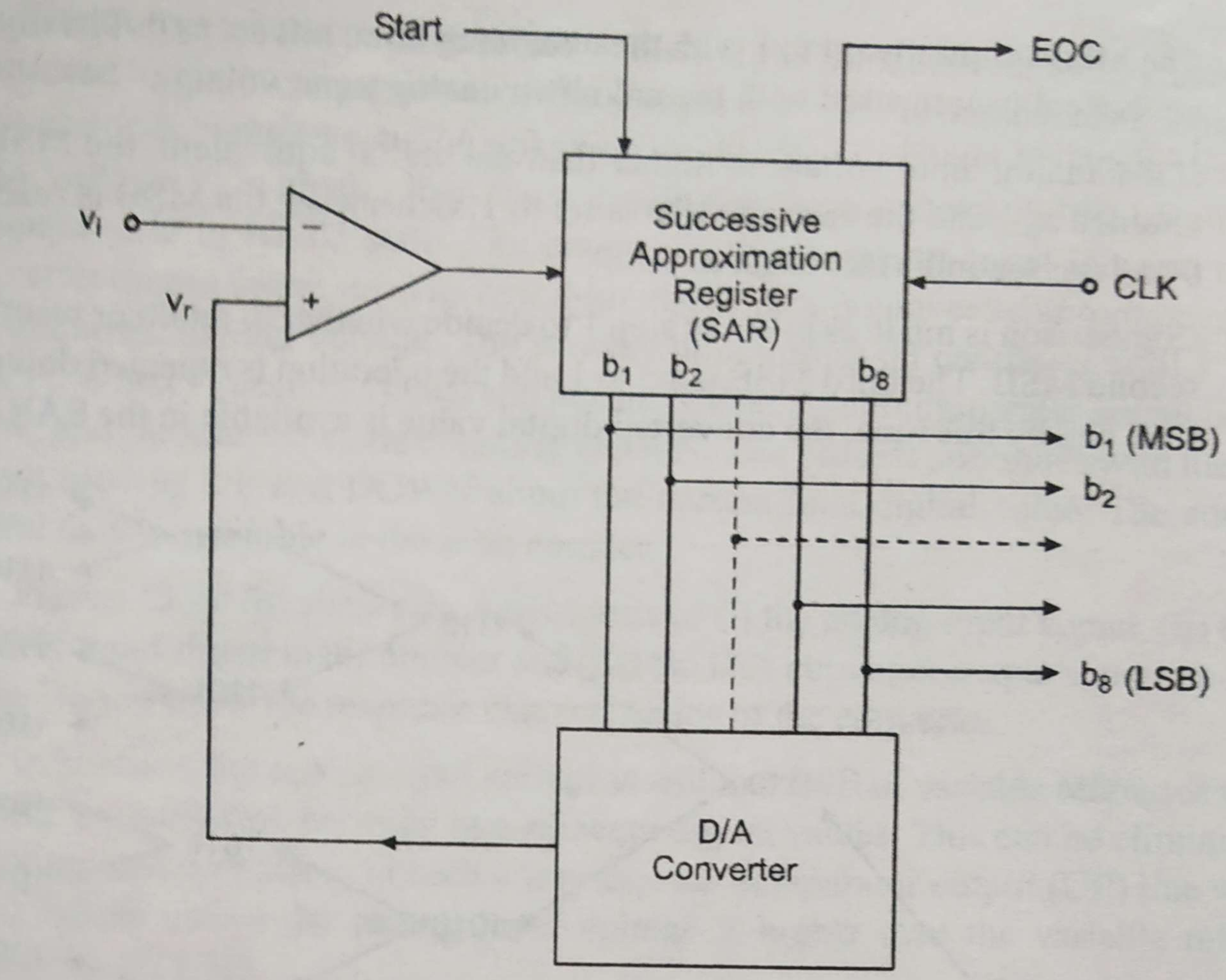


Fig. 13.22 Functional block diagram of a successive approximation type A/D converter

under conversion. The comparator output is used to activate the successive approximation logic of SAR.

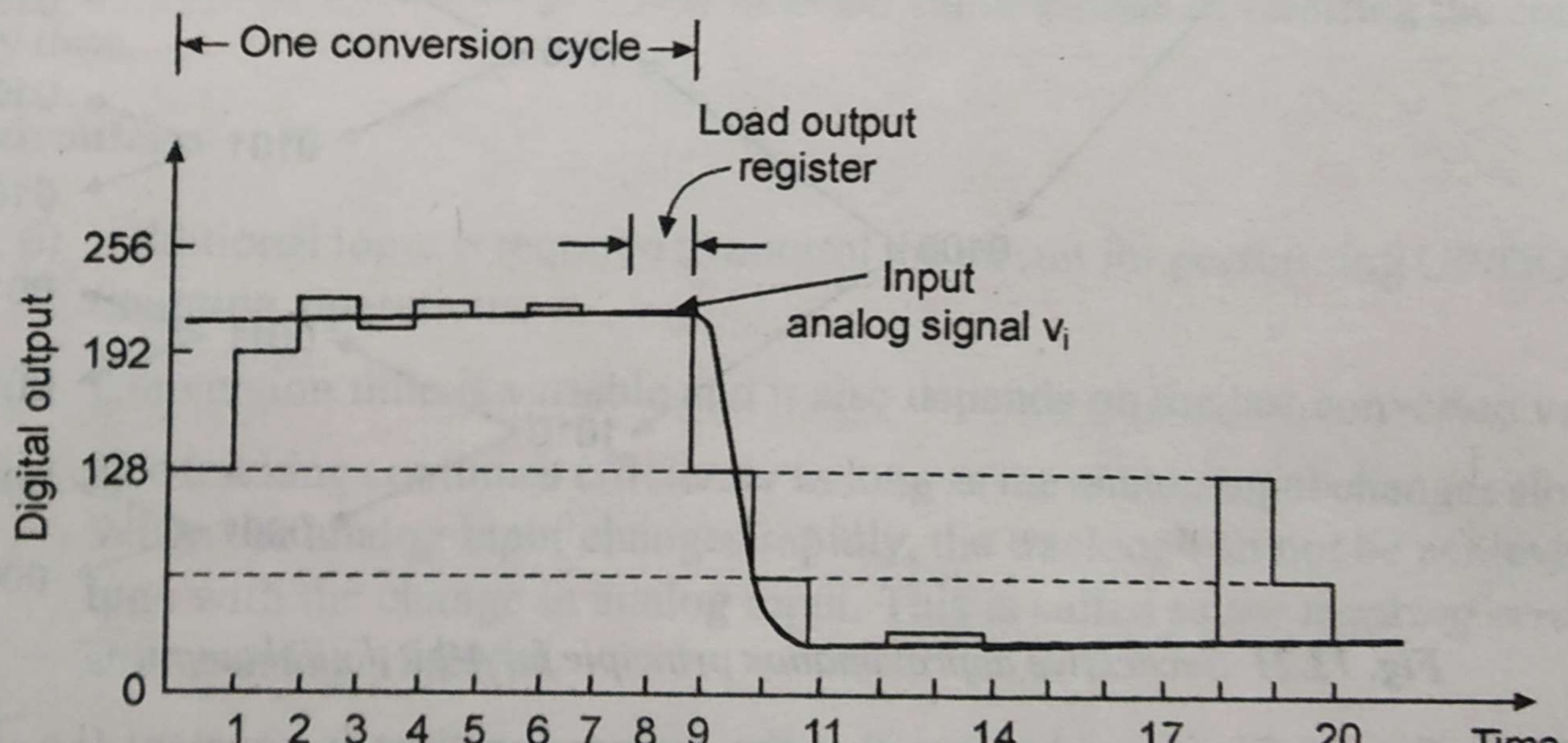


Fig. 13.23 Output response for an analog input

When the START command is applied, the SAR sets the MSB (b_n) of the digital signal, while the other bits are made zero, so that the trial code becomes 1 followed by zeros. For example, for an 8-bit A/D converter the trial code is 10000000. The output of the SAR is converted into analog equivalent V_r and gets compared with the input signal V_i. If V_i is greater than that of the D/A converter output, then the trial code 10000000 is less than the correct digital value. The MSB is retained as 1 and the lower significant bit is made 1 and the testing is repeated. If the analog input V_i is now less than the D/A converter output, then the value 11000000 is greater than the exact digital equivalent. Therefore, the comparator resets the second MSB to 0 and proceeds to the

next most significant bit. This process is repeated for all the remaining lower bits in sequence until all the bit positions are tested. The EOC signal is sent out when all the bits are scanned and the value of D/A converter output just crosses V_i.

Table 13.3 shows the flow of conversion sequence and Fig. 13.23 shows the output response with the associated waveforms. It can be observed that the D/A converter output voltage gets successively closer to the analog input voltage V_i. For an 8-bit A/D converter, it requires 8 pulses to compute the output irrespective of the value of the analog input.

Table 13.3: *Successive approximation conversion sequence*

Correct digital representation	**Successive approximation register (SAR) output V_r ad different stages in the conversion**	**Comparator output**
11010100	10000000	1 (initial output)
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	