AIM: IMPLEMENTATION OF THE GIVEN BOOLEAN FUNCTION USING LOGIC GATES IN BOTH SOP AND POS FORMS.

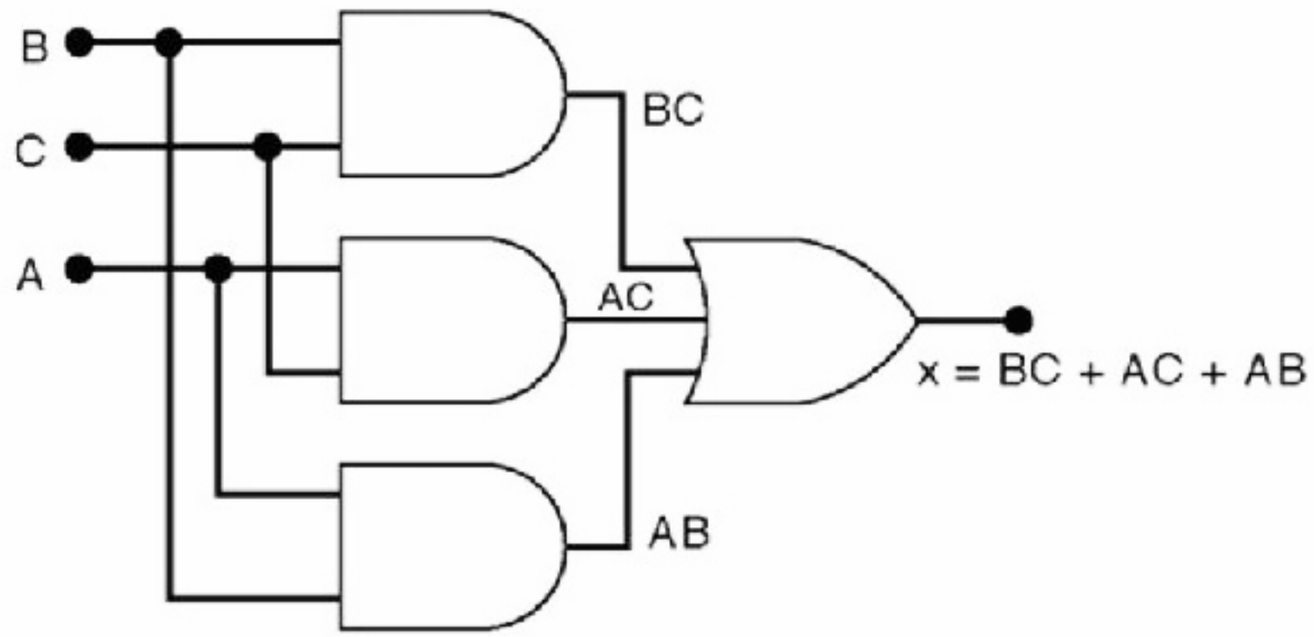
APPARATUS REQUIRED: Power Supply, Digital Trainer, IC's (7404, 7408, 7432) Connecting leads.

BRIEF THEORY: Karnaugh maps are perhaps the most extensively used tool for simplification of Boolean functions. It is mostly used for functions having up to six variables beyond which it becomes very cumbersome. In an n-variable K-map there are 2^n cells. Each cell corresponds to one of the combination of n variable, since there are 2^n combinations of n-variables. Gray code has been used for the identification of cells.

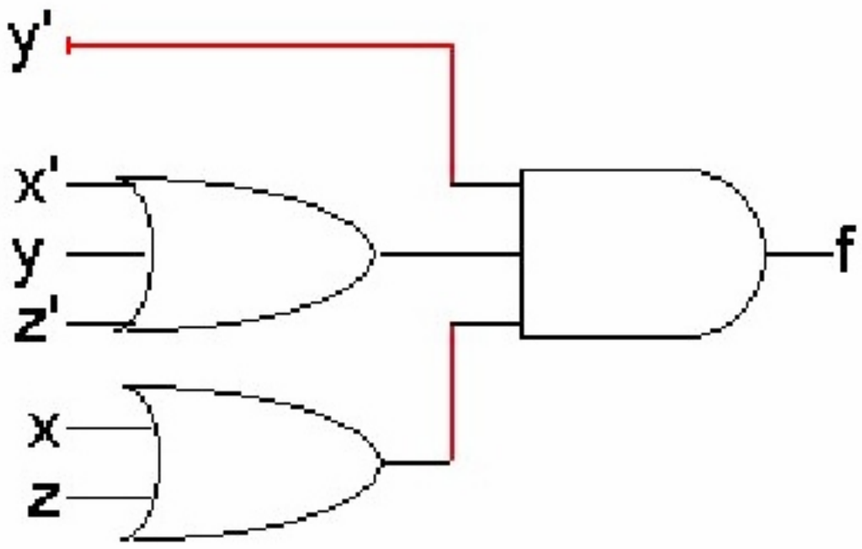
Example- f(A,B,C,D)=A'BC+AB'C+ABC'+ABC (SOP)

Reduced form is BC+AC+ABand POS form is f(X,Y,Z)= Y'(X'+Y+Z')(X+Z)

CIRCUIT DIAGRAM



SOP form



PROCEDURE:

(a) With given equation in SOP/POS form first of all draw a K-map.
(b) Enter the values of the O/P variable in each cell corresponding to its Min/Max term.
(c) Make group of adjacent ones.
(d) From group write the minimized equation.
(e) Design the ckt. of minimized equation & verify the truth table.

RESULT/CONCLUSION: Implementation of SOP and POS form is obtained with AND and OR gates.

PRECAUTIONS:

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The V_{cc} and ground should be applied carefully at the specified pin only.