Ripple Counters with modulus $< 2^n$

The basic ripple counter is limited to a MOD-number that is equal to 2^n, where n is the number of flip-flops. This value is actually the maximum MOD-number that can be obtained using n-flip-flops. The basic counter can be modified to produce MOD-number less than 2^n by allowing the counter to skip states that are normally a part of the counting sequence.

To construct any MOD-N counter, the following method can be used

1. Find the number of flip-flop (n) required for the desired MOD number - N using the equation

$$2^{n-1} \leq N \leq 2^n$$

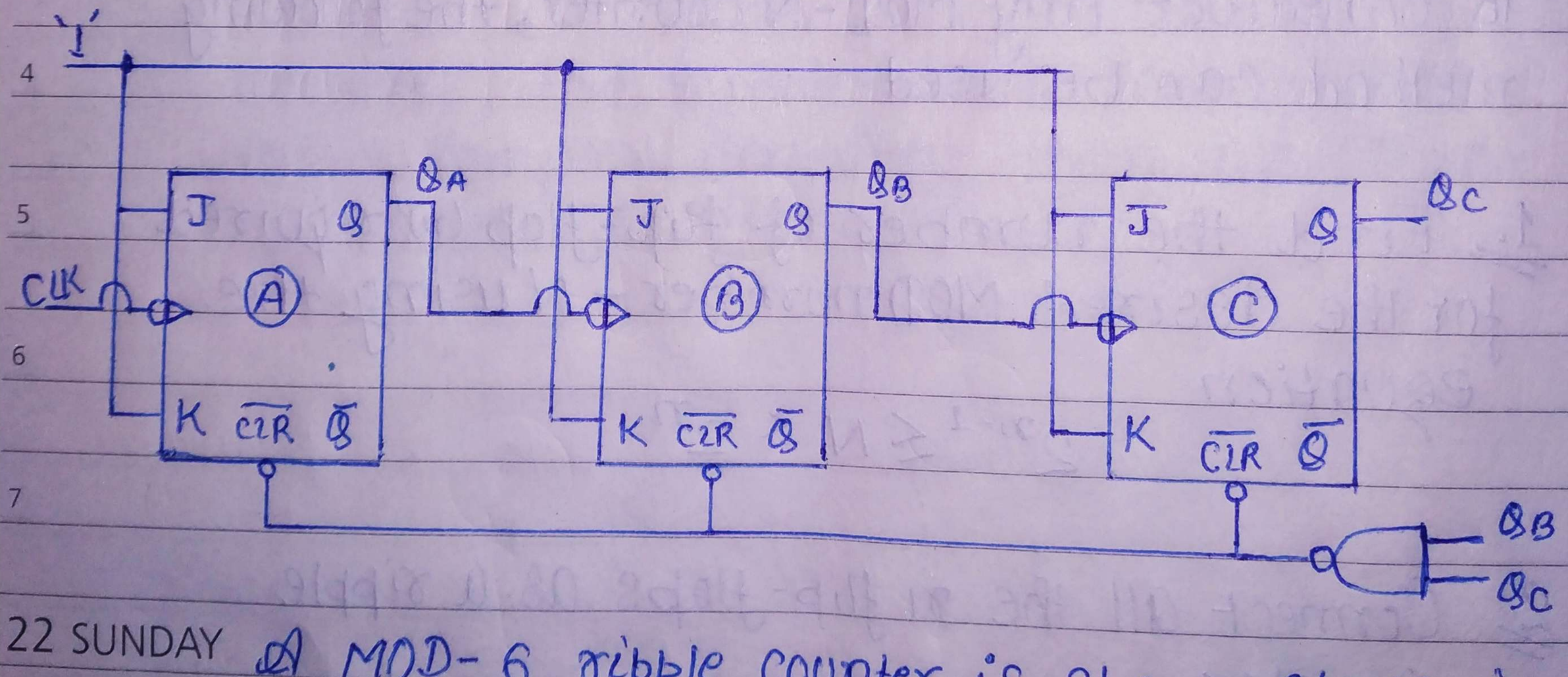
2. Connect all the n flip-flops as a ripple counter
3. Find the binary number for N.
4. Connect all flip-flop output, for which $Q = 1$ when the count is N, as input to NAND gate.
5. Connect the NAND gate output to the CLEAR input of each flip-flop.

When the Counter reaches its N^{th} state, the output of the NAND gate goes LOW, resetting all flip-flops to 0. So, the Counter counts from 0 through N-1, having N-States.

A MOD-6 Counter can be designed using above mentioned procedure. So, for MOD-6 $N = 6$, therefore no. of flip-flop will be

$$2^{n-1} \leq 6 \leq 2^n$$

$n = 3$, satisfyes the inequality



22 SUNDAY A MOD-6 ripple Counter is shown above, in absence of NAND gate, this Counter will function as a MOD-8 binary Counter, ~~which counts~~ The presence of NAND alters the sequence as the output of NAND gate is connected

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to the CLEAR inputs of each flip-flop. As long as the NAND gate output is High, it will have no effect on the counter, when the NAND gate output goes LOW, it will clear all flip-flop and the counter immediately goes to the 000 State.

Therefore, the counting sequence is 000 → 001 → 010 → 011 → 100 → 101 → 000 ....

Although the counter does go to the 110 state, it remains there only for a few nano seconds before it recycles to 000. As at 110 State $Q_B = Q_C = 1$, So output of NAND will be '0', So, all flip-flop will reset.

Thus, we can say that this counter counts from 000 to 101 and then recycles to 000. It essentially skips 110 and 111 States going only through Six different States; thus it is a MOD-6 counter.

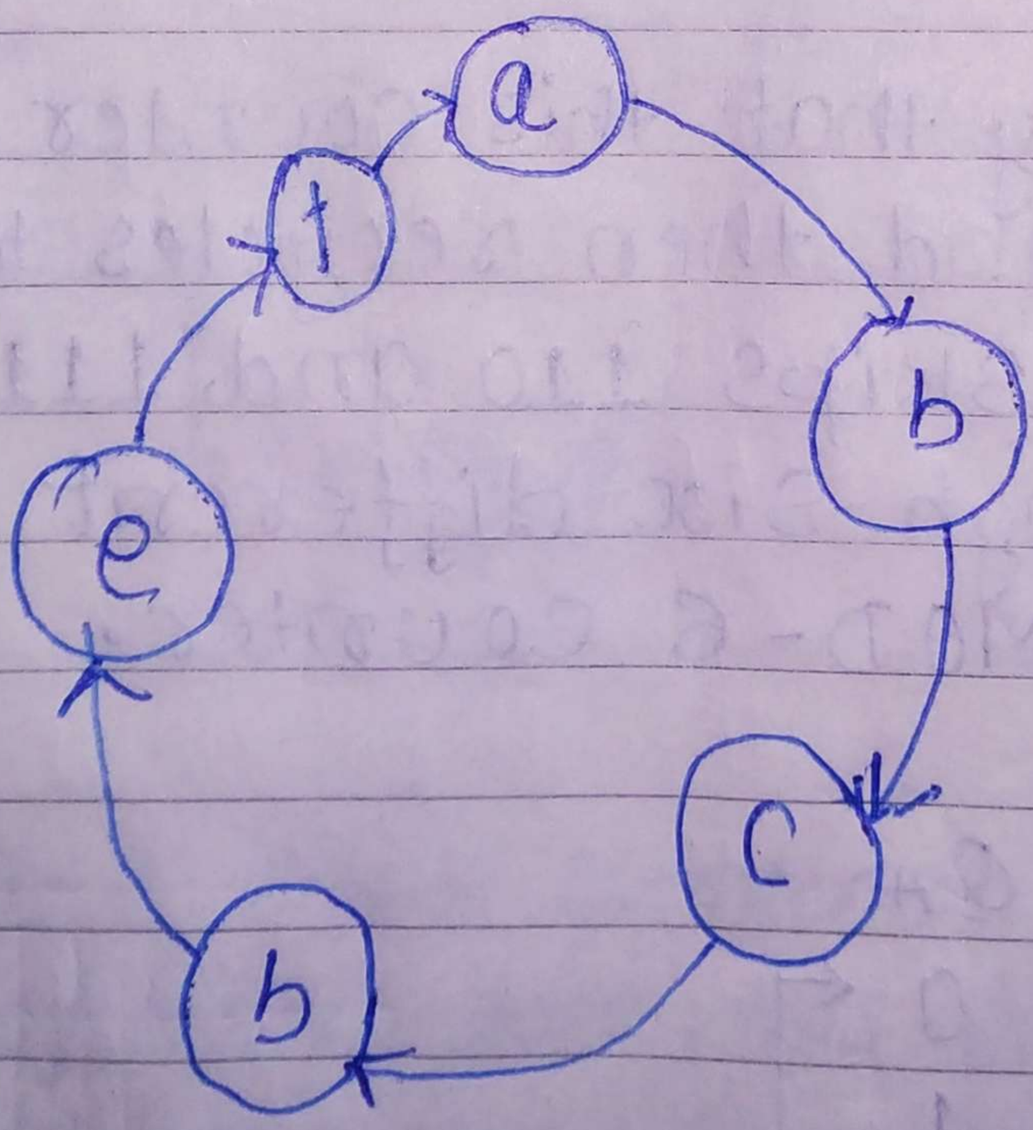
CLK	Q_C	Q_B	Q_A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1

Synchronous Counter with MOD-6

In order to design a MOD-6 Counter with six states, the number of flip-flops required is three. This is found from the equation $2^{n-1} \leq N \leq 2^n$, where $N = 6$, the number of states present in the MOD-6 Counter.

Let us assume that the MOD-6 counter has six states, viz a, b, c, d, e and f.

Step 1 :- State diagram :- The state diagram for the MOD-6 counter can be drawn as shown in figure. Here, it is assumed that



the state transition from one state to another takes place when the clock pulse is asserted;

When the clock is unasserted, the counter remains in the present state.

Step 2:- State table :- From the state diagram one can draw Present State to Next State table as shown below

Present state	Next state
a	b
b	c
c	d
d	e
e	f
f	a

Step3:- State assignment :- Let us assign three State variables to state a, b, c, d, e and f as

Present State (PS)			(NS) Next State		
q_2	q_1	q_0	Q_2	Q_1	Q_0
a	0	0	0	0	1
b	0	0	1	0	1	0
c	0	1	0	0	1	1
d	0	1	1	1	0	0
e	1	0	0	1	0	1
f	1	0	1	0	0	0

Step 4:- Excitation table :- The J-K flip-flop is selected for the counter design because it results in a simplified circuit. The

excitation table having entries for flip-flop inputs J_2K_2, J_1K_1 and J_0K_0. It can be formed from PS-NS table and excitation table of JK flip-flop.

Present State			Next State			Excitation inputs					
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	1	0	d	0	d	1	d
0	0	1	0	1	0	0	d	1	d	d	1
0	1	0	0	1	1	0	d	d	0	1	d
0	1	1	1	0	0	1	d	d	1	d	1
1	0	0	1	0	1	d	0	0	d	1	d
1	0	1	0	0	0	d	1	0	d	d	1
1	1	0	d	d	d	d	d	d	d	d	d
1	1	1	d	d	d	d	d	d	d	d	d

Excitation table for MOD-6 Counter

Step 5 :- Excitation maps :- The excitation maps for J_2, K_2, J_1, K_1, J_0 & K_0 inputs of the counter can be drawn from excitation table of MOD-6 Counter using K-map as

Q_2 \ Q_1Q_0	00	01	11	10
0	0	0	1	0
1	d	d	d	d

$J_2 = Q_1Q_0$

Q_2 \ Q_1Q_0	00	01	11	10
0	d	d	d	d
1	0	1	d	d

$K_2 = Q_0$

Q_2 \ Q_1Q_0	00	01	11	10
0	0	1	d	d
1	0	0	d	d

$J_1 = \bar{Q}_2 Q_0$

Q_2 \ Q_1Q_0	00	01	11	10
0	d	d	1	0
1	d	d	d	d

$K_1 = Q_0$

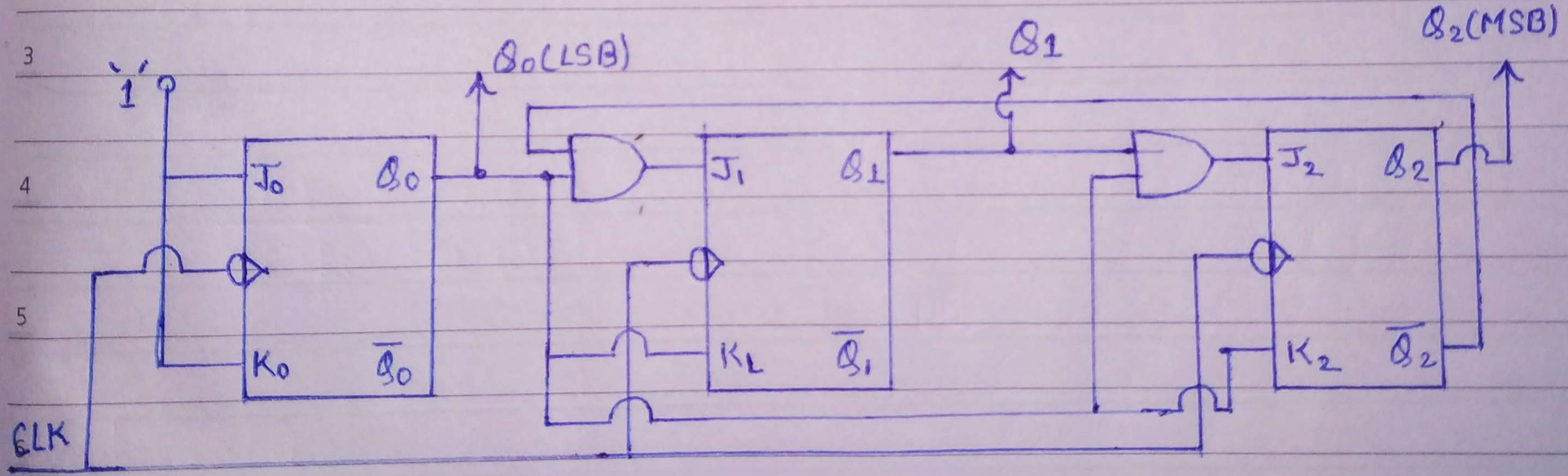
Q_2 \ Q_1Q_0	00	01	11	10
0	1	d	d	1
1	1	d	d	d

$J_0 = 1$

Q_2 \ Q_1Q_0	00	01	11	10
0	d	1	1	d
1	d	1	d	d

$K_0 = 1$

Step-6 : Schematic diagram :- using the above excitation equation, the circuit diagram for the MOD-6 counter can be drawn as



MOD-6 Synchronous Counter