8.5 COUNTER ICs

8.5.1 IC 7493—4-bit Binary Ripple Counter

IC 7493 is a 4-bit binary ripple counter that consists of four master–slave flip-flops as shown in Fig. 8.6. These four flip-flops are internally connected to provide a divide-by-2 and divide-by-8-bit counter. The reset inputs R_1 and R_2 are used to reset the counter to 0000. Since the output Q_A from flip-flop A is not internally connected to the succeeding flip-flops, the counter may be operated in two independent modes as shown below.

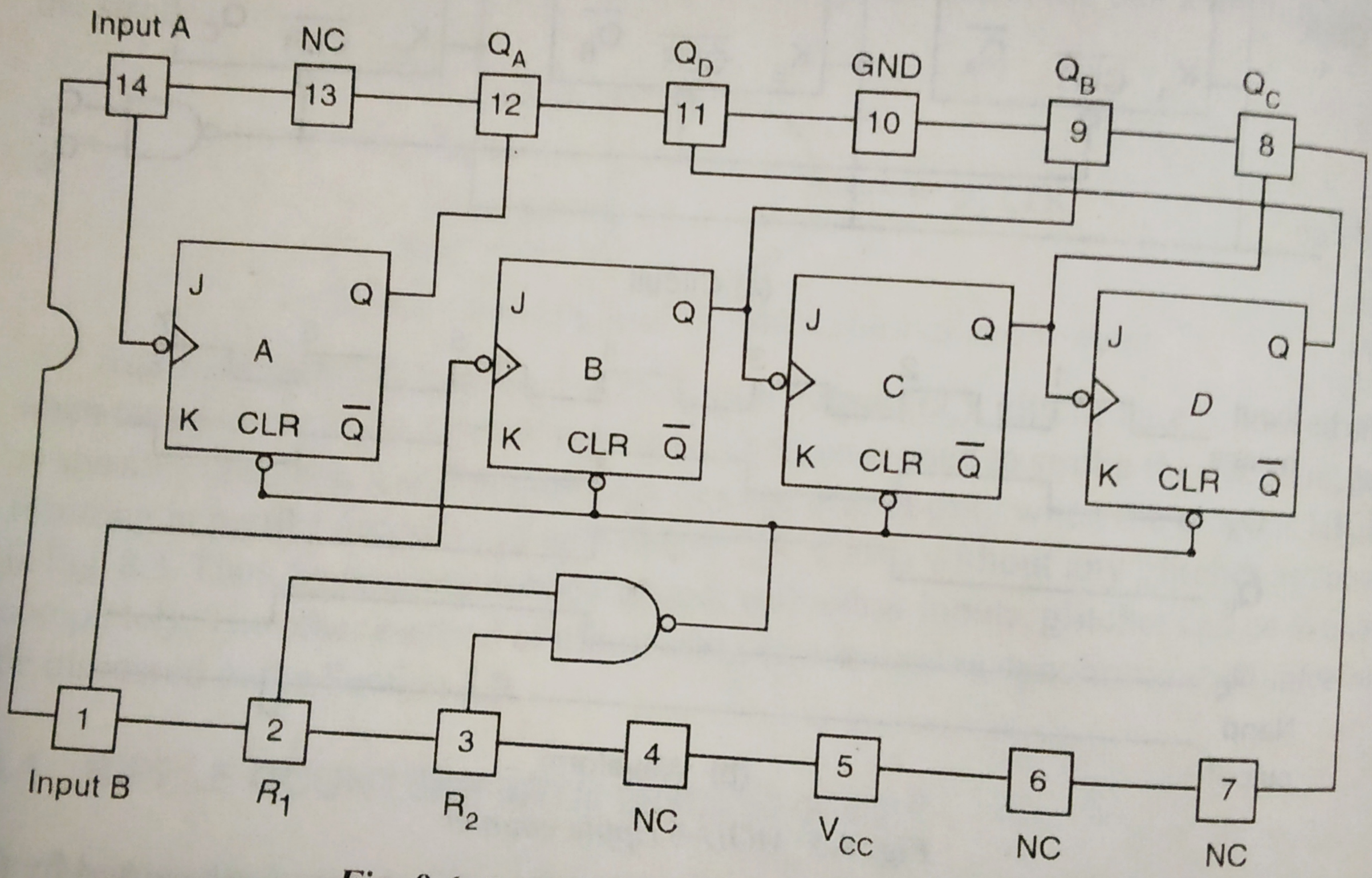

Fig. 8.6 7493—4-bit binary ripple counter

1. When used as a 4-bit ripple counter, output Q_A must be externally connected to input *B*. The input pulses are applied to input *A*. Simultaneous divisions of 2, 4, 8 and 16 are performed at the Q_A, Q_B, Q_C, and Q_D outputs. The truth table for this connection is given in Table 8.2.
2. When used as a 3-bit ripple counter, the input count pulses are applied to input *B*. Simultaneous frequency divisions of 2, 4 and 8 are performed at Q_B, Q_C and Q_D outputs. Independent use of flip-flop *A* is available if the reset function coincides with the reset of the 3-bit ripple counter.

Table 8.2 Truth table for 7493 —4-bit binary ripple counter

Mode -1 (divide-by-16)				Mode-2 (divide-by-8)		
Q_D	Q_C	Q_B	Q_A	Q_D	Q_C	Q_B
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	1	0	0
0	1	0	1	1	0	1
0	1	1	0	1	1	0
0	1	1	1	1	1	1
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			
0	0	0	0			

8.5.2 IC 7490 — Decade Counter

IC 7490 is a decade counter (MOD-10), which consists of four master–slave flip-flops internally connected to provide a divide-by-2 counter and a divide-by-5 counter, as shown in Fig. 8.7. The reset inputs R_1 and R_2 are used to reset the counter to 0000 and the set inputs S_1 and S_2 are used to set the counter to 1001. Since the output Q_A from flip-flop A is not internally connected to the succeeding stages, the counter can be operated in two independent count modes.

1. When used as a BCD counter, the B input must be externally connected to the Q_A output. The input A receives the incoming pulses, and a count sequence is obtained in accordance with the BCD count sequence as shown in, Table 8.3. Two gated inputs are provided to reset the counter to 0. In addition, two more inputs are also provided to set to a BCD count of 9 for 9's complement decimal applications.
2. No external interconnections are necessary when it is required to function as a a divide-by-2 counter and a divide-by-5 counter. Flip-flop A is used as a binary element for the divide-by-2 function. The B input is used to obtain binary divide-by-5 operation at the Q_B, Q_C and Q_D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

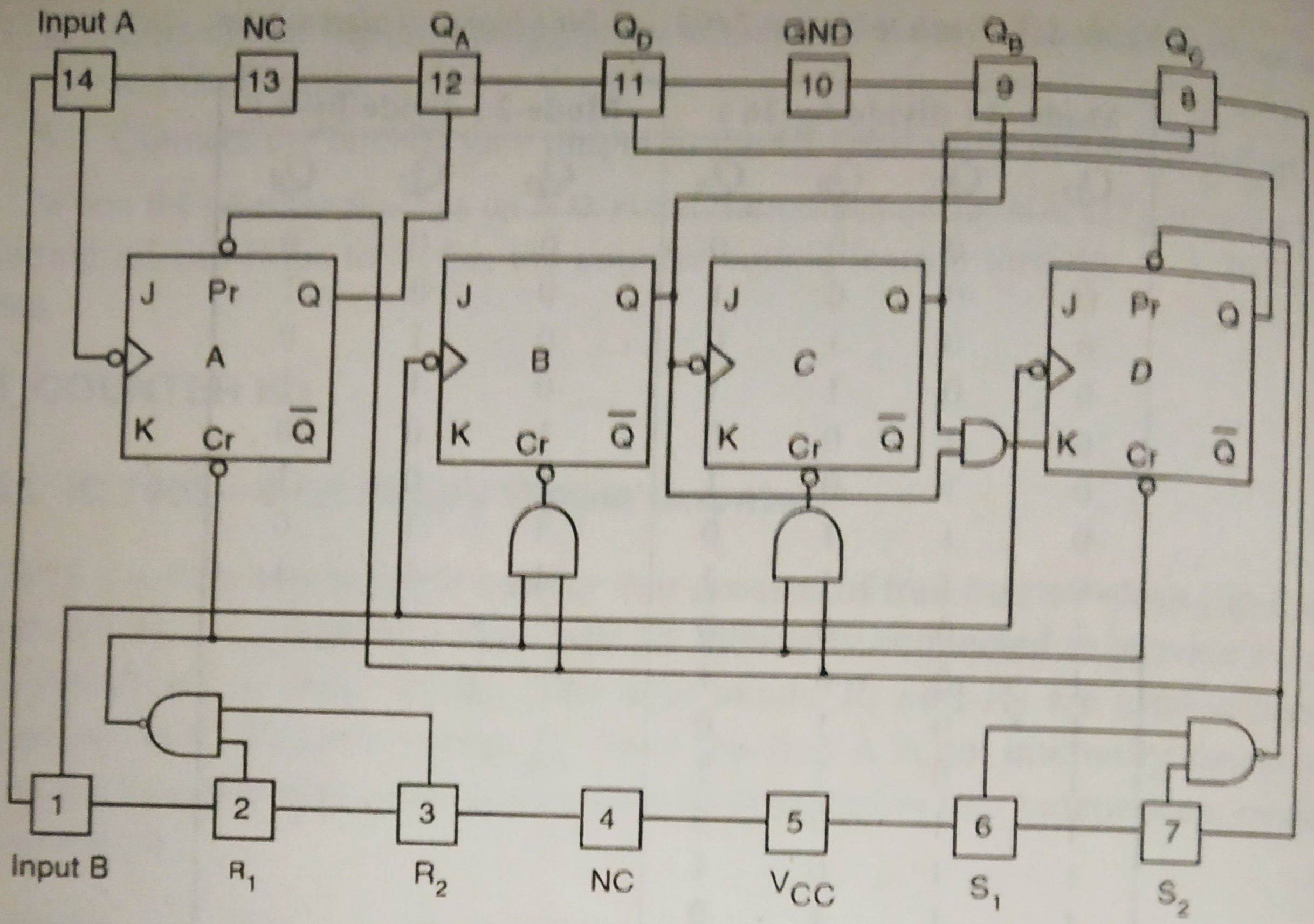

Fig. 8.7 *7490—decade counter*

Table 8.3 *Truth table for 7490—decade counter*

Mode -1 (divide-by-10)				Mode-2 (divide-by-5)		
Q_D	Q_C	Q_B	Q_A	Q_D	Q_C	Q_B
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	1	0	0
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			

ASYNCHRONOUS