# Purnea College of Engineering, Purnea

## Assignment-5 (Digital circuit)

Branch – ECE, 4th sem.

Que!- 1. Device used to convert a binary number to 7-segment display format is called —

(a) Multiplexer (b) Encoder (c) Decoder (d) Register

Que!-2. An asynchronous counter differs from synchronous counter with —

(a) the no. of states (b) method of clocking

(c) the type of flip-flop (d) the value of modulus

Que!-3. Asynchronous inputs in a flip-flop —

(a) S, R (b) S, $\overline{PR}$ (c) $\overline{CLR}$, $\overline{PR}$ (d) R, $\overline{CLR}$

Que!-4. Which of the following logic family is fastest —

(a) TTL (b) DTL (c) CMOS (d) ECL

Que!-5 Which of the following has high fan-out —

(a) TTL (b) DTL (c) CMOS (d) ECL

Que!-6 very large scale integration (VLSI) consist of

(a) 10 to 100 gates (b) 100 to 1000 gates (c) more than 1000 gates

Que!-7. Figure of merit of a digital IC is given by .....?

Que!-8. Race around condition in J-K flip-flop can be avoided if

(a) $t_p < \Delta t < T$ (b) $t_p > \Delta t > T$ (c) $t_p = T$ (d) None of these

Que!-9. Implement the following multi-output combinational logic circuit using 4-to-16 decoder:

$F_1 = \Sigma_m(1,2,4,7,8,11,12,13)$, $F_2 = \Sigma_m(2,3,9,11)$, $F_3 = \Sigma_m(2,4,8)$

$F_4 = \Sigma_m(10,12,13,14)$

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