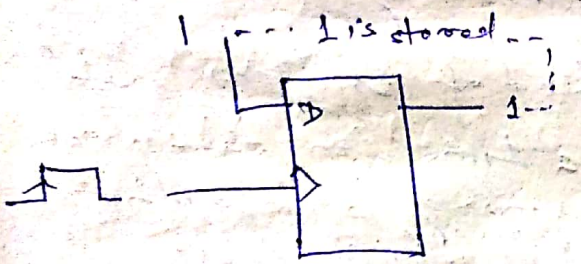
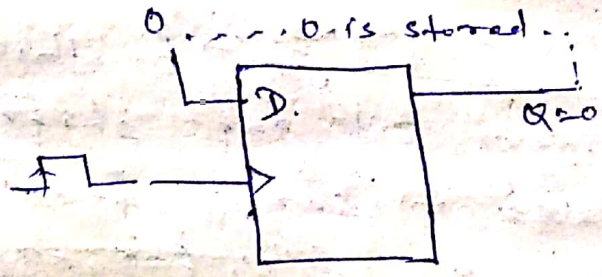
Register

A Register is a digital circuit with two basic function : data storage and data movement. Basically, a register is a group of flip-flops suitable for storing binary information. Each flip-flop is a binary cell capable of storing one bit of information. An n-bit register has n-flip-flop and capable to store n-bit binary information. A register is a sequential ckt and a building block of digital system like multipliers, dividers, memories, microprocessor etc.

The fig. 1(a) & (b) given below is simple ~~com~~ example and a concept of storing 1-bit (either 0 or 1).



When a 1 is applied to input D and a clock +ve edge is given to clock input, then a 1 is appeared at Q and remains same if is set.



When 0 is applied to D-input then at +ve edge of clock pulse, 0 appears at Q and remains same ~~until~~ if it is at Reset.

Register

- Memory register
- Shift Register

(i) Memory Register :→ A Register that can stores the binary bit information is known as memory register.

(ii) Shift Register :→ A register that is capable to shift the binary information either to left or to right is known as shift register. A shift register gives the permission to the stored data to move from a particular location to some other location. In a shift register a no. of flip-flops are connected in such a manner that the binary bit entered into register, shifted one position to another position.

There are two methods of shifting — ① Serial shifting
② Parallel shifting.

① Serial shifting :→ In this method of shifting each binary bit get shift at a time for each clock pulse in serial fashion, beginning with either MSB or LSB. For example, A 4-bit serial register requires four clock pulses to shift a bit from input to output.

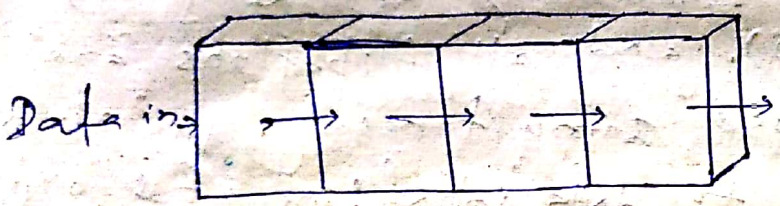
②. Parallel shifting :→ In parallel shift operation, all the data at input (or o/p) get shifted simultaneously during a single clock pulse.

Hence, parallel shifting method is faster than serial shifting.

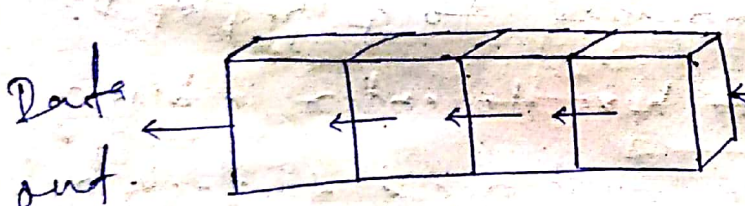
The shift registers are classified as below on the basis that how the binary information entered and how binary information out.

i) Serial-in-Serial Out (SISO).
ii) Serial-in-parallel out (SIPO)
iii) Parallel-in-Serial Out (PISO)
iv) Parallel-in-Parallel out (PIPO).

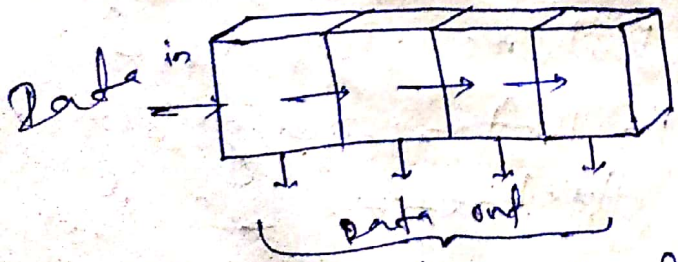
The fig. as shown below, are the block diagram of four types of shift register



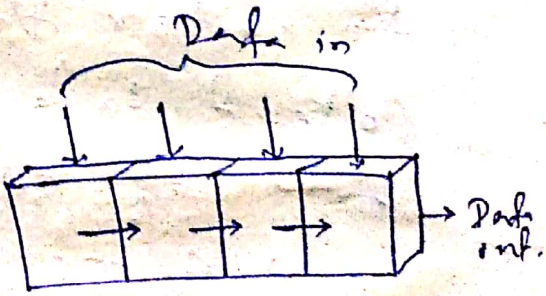
Serial in / serial out (shift-Right)



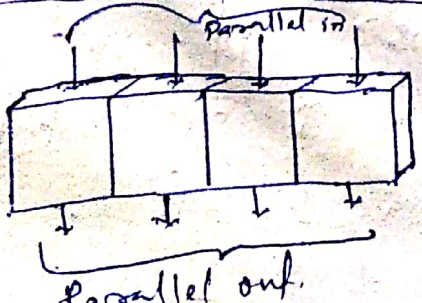
Serial in / shift left / serial o/p.



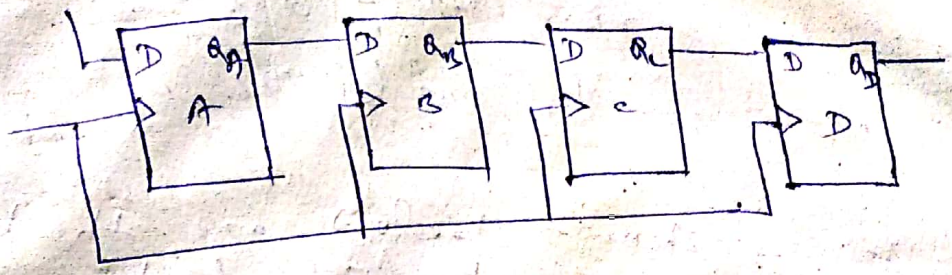
Serial in / Parallel out.



Parallel in / serial out.



4-bit serial in/serial out Register :-



The above fig. shows a 4-bit serial in/serial out shift register, consisting of 4-D-flip flops A, B, C and D. Initially, all the flip-flops are at RESET (0), and all flip-flops are +ve edge triggered simultaneously. The o/p Q_A of A is connected to data input line of B, o/p of B (Q_B) is connected to input of C and o/p Q_C of C is connected to flip-flop D.

Let us consider, We have to enter a binary data 1101, then we must need 4-clock pulses to enter the data 1101 and if we want collect data at fourth flip-flop or all bits at right side, then again we need 4 more clock pulses. This fact can be understood in better way by taking following illustration as below.

Here we start to enter data 1101 from right most (LSB) bit. we put LSB bit 1 at data line D of flip-flop A. When data input to A is 1, at the same time inputs for B, C and D are 0. Now,

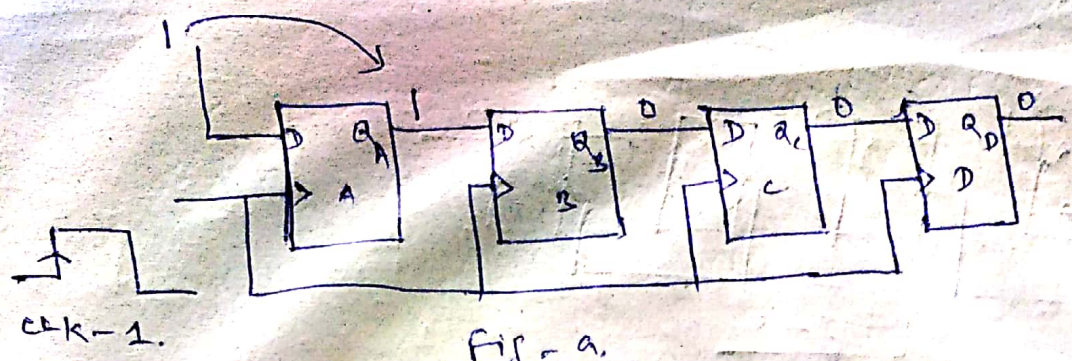


fig - a.

as soon as 1st ↑ clock pulse is applied, all the flip-flops are triggered simultaneously. The data input D=1 for A is ~~shifted~~ stored in A, and data input to B which is Q_A=0 is shifted to flip-flop B and stored, and stored bit 0 in B is shifted to flip-flop C and previous bit Q_c=0, which was stored in C is shifted into flip-flop D. It is shown in fig-(b)

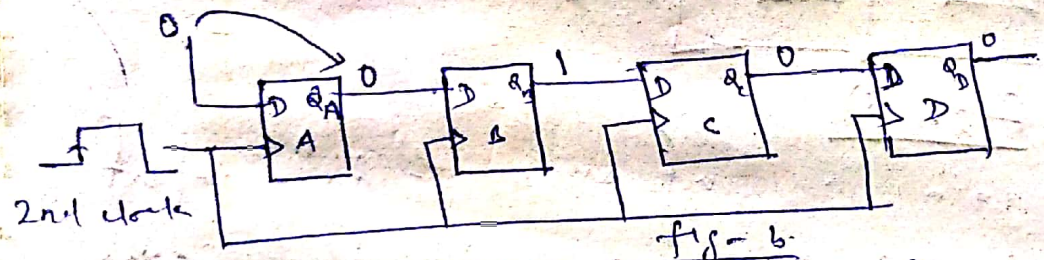


fig - b.

Now, again, we put D=0 at A, then input of B is 1, input of C is 0, input of D is 0. As soon as 2nd clock is applied, the data input D=0 is ~~store shifte~~ stored in A i.e flip-flop A is reset and flip-flop B is set because, before applying clock pulse D=1 for B. Thus, 1 is shifted from A to B and stored into B. Similarly Q_c=0 and Q_D=0 because previously they ~~are of~~ 0; have the data

input as 0.

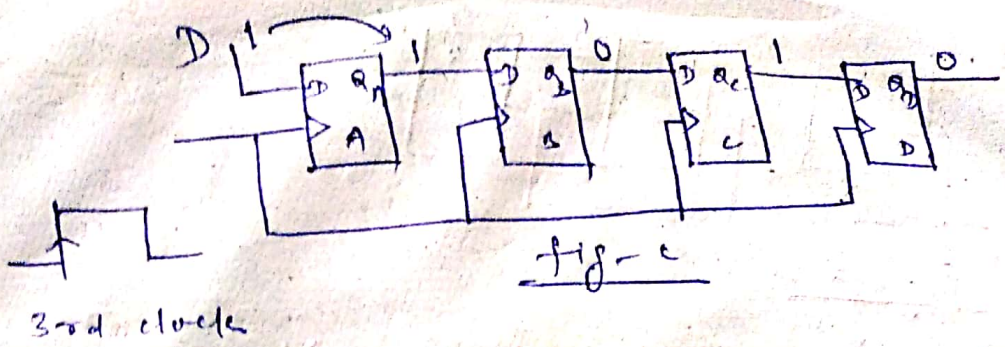


fig-c

Now, we put D=1 of A. At the same time D=0 for B, D=1, for C and D=0 for D. When 3rd clock pulse is applied, flip-flop A become set and store 1. i.e stored data Q_A=D is shifted to B and stored. Similarly, flip-flop C is set and D is reset which shown in fig-c.

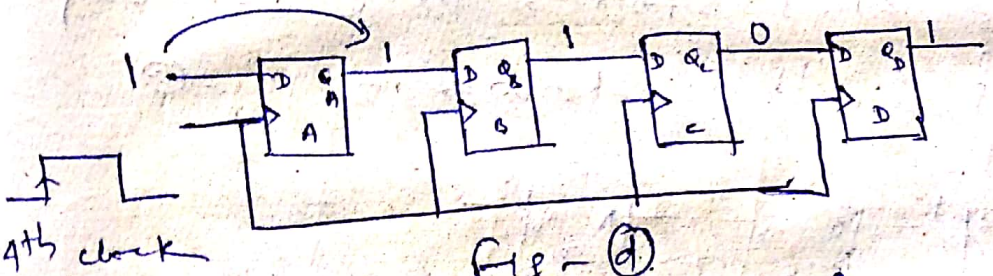


Fig-(d)

Now, again we put MSB of data input to flip-flop A i.e D=1 for A. At the same time D=1 for B, D=0 for C and D=1 for D. As soon as ~~clock~~ 4th clock is applied, A become set and stored bit 1 in A is shifted to B, stored bit 0 in B is shifted to C and stored bit 1 in C is shifted to flip-flop D. Thus, all the bits of 1101 now has been entered in register ~~at~~ after 4th clock pulse which is shown in fig-(d).