D.E.

SEQUENTIAL CIRCUIT

The circuit which output does not depend only on the present value of input but also on the past output, is called sequential circuit. Thus in a sequential ckt some part of output is fed-back to the input through a feedback path (usually memory element). Such a system is called closed loop system.

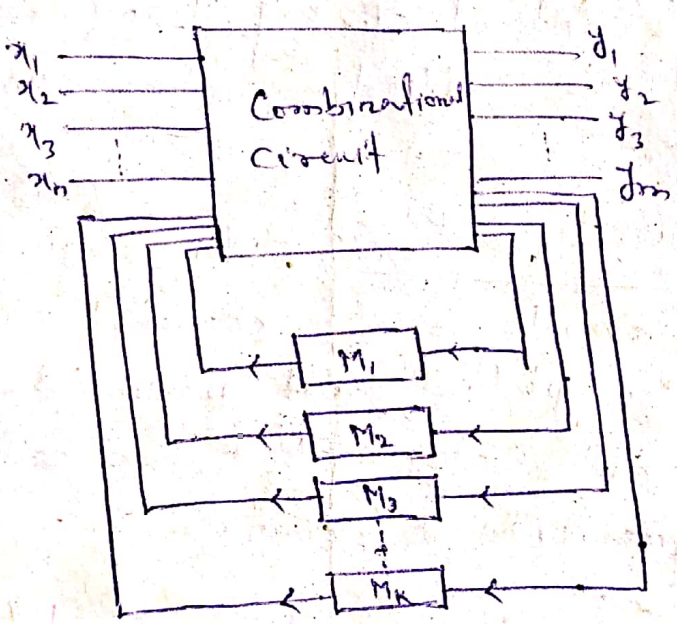
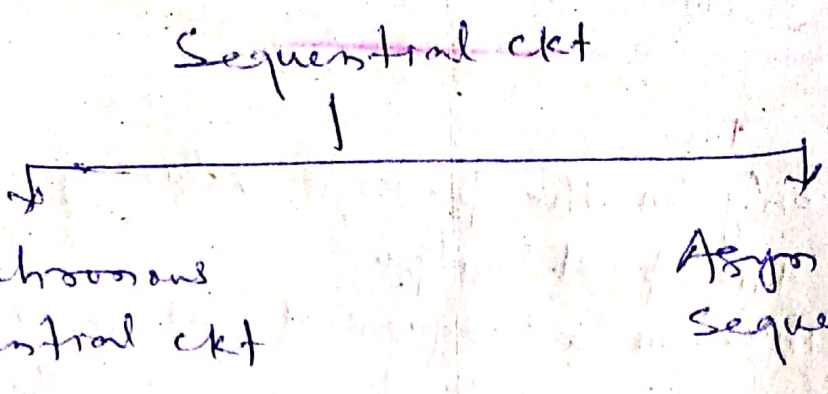


Fig-1

The above fig-1 represent a sequential ckt with $x_1, x_2, x_3, \ldots x_n$ as inputs, $y_1, y_2, y_3 \ldots y_m$ as outputs and $M_1, M_2, M_3, \ldots M_3$ as memory element constitutes the feedback-path. It is to be noted that Combinational circuit is faster than sequential circuit because, Combinational circuit does not need any memory element or o/p does not depend upon any sequence of past output but only depends upon present input value.



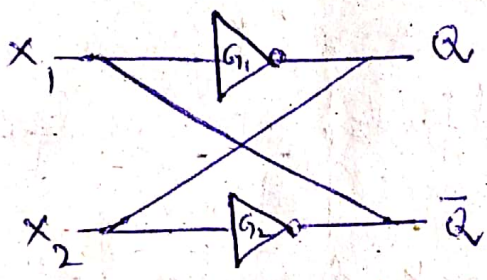
~~Sequential~~

Synchronous sequential ckt :- The sequential ckt in which the input is transferred only when an external control clock pulses (or triggering) is applied is called synchronous sequential ckt.

Asynchronous sequential ckt :- The sequential circuit in which events are occured when one event is completed and no need of any control triggering pulses, is called asynchronous sequential circuit.

Note:- i) Asynchronous circuit is faster than Synchronous becaus there is no need to Synchronise the inputs with clock pulses. But, asynchronous ckt is unstable.

Latch :- The simplest kind of sequential circuit has only two states as "HIGH" and "LOW". It is a memory cell that is capable to store only one bit at a time either '0' or 1. Such type of sequential circuit is called "Latch". A latch is a bistable multivibrator that can store either '0' or 1 at a particular time. This is a basic unit of memory. The basic latch consist of two inverters cross-connected of their outputs as shown in figure as below ——



If $X_1 = 0$ then $Q = \bar{0} = 1$ and $X_2 = 1$, $\bar{Q} = \bar{1} = 0$. The circuit remains latched in same state untill X_1 ~~is~~ does not changed. Thus, circuit can store one-bit binary.

Flip-flop :- The basic operation of latch can be modified by providing additional clock pulse (or triggering) that determines when the state of latch to be changed. Thus, a latch synchronised with additional clock pulse is called flip-flop.

Types of latches.

i) S-R latch (flip-flop)

ii) J-K " "

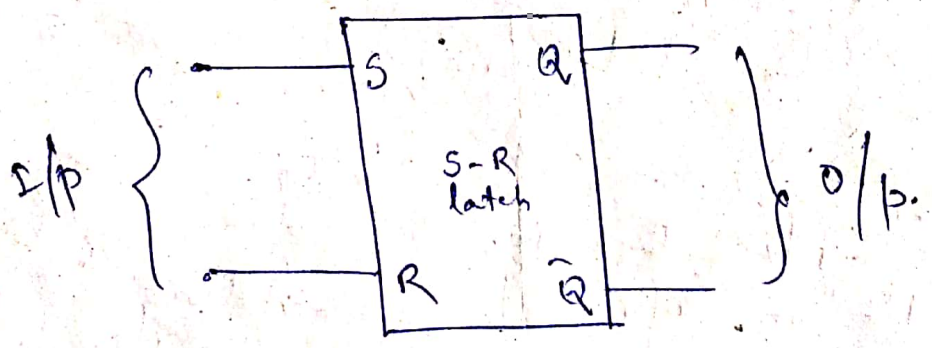
iii) D " "

iv) T " "

v) Master-slave "

Note:- A flip-flop provides -ve feedback.

i) S-R (Set-Reset):- S-R latch can be implemented by using two NOR gates or two NAND gates. An S-R latch has two inputs as 'Set' and 'Reset' (Synchronous input) and two outputs. The outputs are complement of each other as Q and $\bar{Q}$. The basic block diagram of S-R latch is shown in fig-1 as below —



NOR realized S-R latch :- NOR realized S-R latch is implimented by using two NOR gates connected as shown in fig-2. NOR realized S-R latch is also called "ACTIVE HIGH" latch.

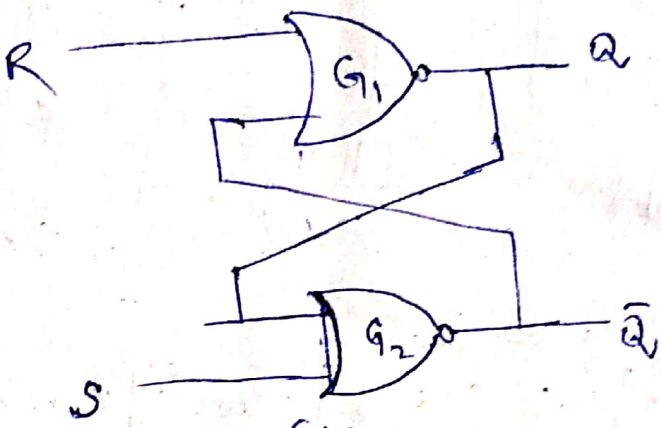


Fig-2

Here the output of G_1 is fed-back to one input to G_2 and output of G_2 is fed-back to one input of G_1, i.e o/p of each other are crossed coupled to their one input line. The action of this ckt and how it can store one-bit binary, can be understood by following truth table —

S	R	Q_{n+1}	$\bar{Q}_{n+1}$	Action
0	0	Q_n	$\bar{Q}_n$	No change
0	1	0	1	Reset
1	0	1	0	set
1	1	?	?	Invalid

When clock pulse is applied, ckt is called flip-flop.

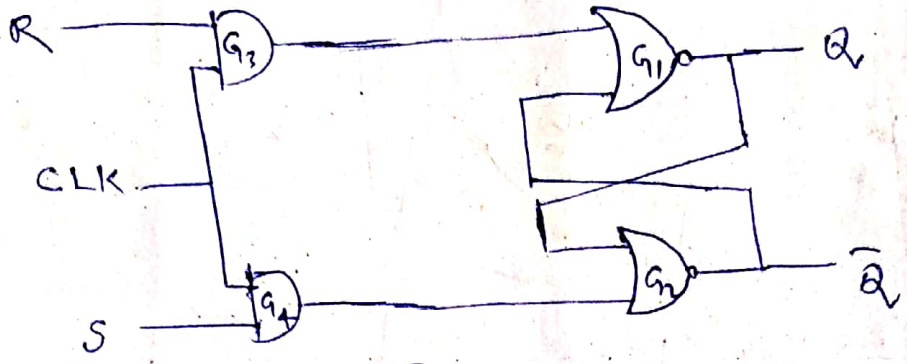


Fig - 3

CLK	S	R	Q_{n+1}	$\bar{Q}_{n+1}$	Actions
0	0	0	Q_n	$\bar{Q}_n$	NC
0	0	1	Q_n	$\bar{Q}_n$	NC
0	1	0	Q_n	$\bar{Q}_n$	NC
0	1	1	Q_n	$\bar{Q}_n$	NC
1	0	0	Q_n	$\bar{Q}_n$	NC
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	?	?	Forbidden (Invalid).

Fig - 4

NAND realized $\bar{S}$-$\bar{R}$ latch :- NAND realized $\bar{S}$-$\bar{R}$ latch is also called ACTIVE LOW latch because on of its two inputs when goes to Low, ckt become active which is illusted by truth table. To implement $\bar{S}$-$\bar{R}$ latch, two NAND gates are used and their outputs are cross-coupled to their one input as shown in fig-(5)

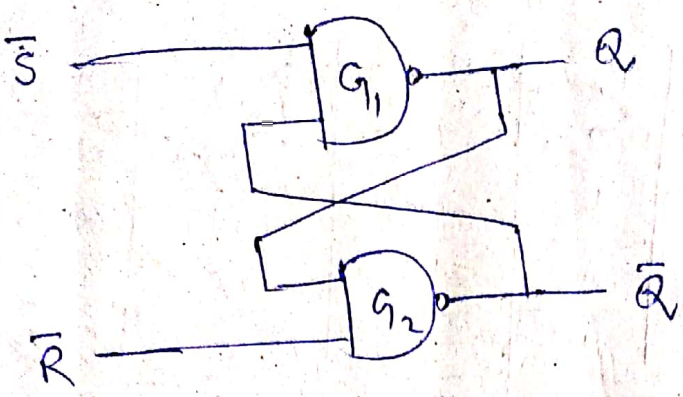
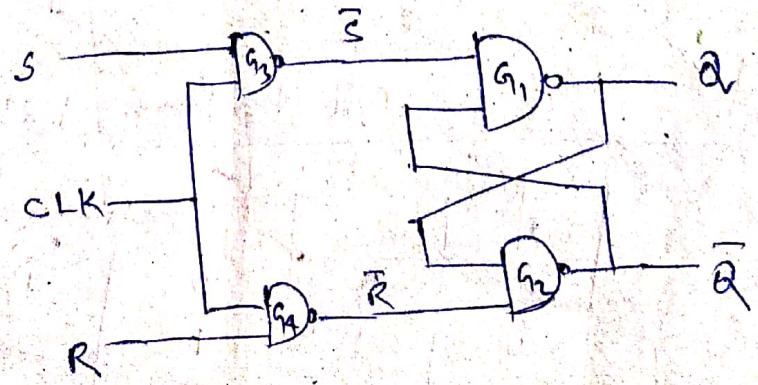


fig-(5)

The action of $\bar{S}$-$\bar{R}$ latch can be understood in better way by following truth table—

$\bar{S}$	$\bar{R}$	Q_{n+1}	$\bar{Q}_{n+1}$	Action
0	0	?	?	Forbidden
0	1	1	0	set
1	0	0	1	Reset
1	1	Q_n	$\bar{Q}_n$	NC.

When clock pulse is applied, ckt is termed as flip-flop. $\bar{S}$-$\bar{R}$ flip-flop is shown in fig-6 as below —



Present-Next state table for S-R latch

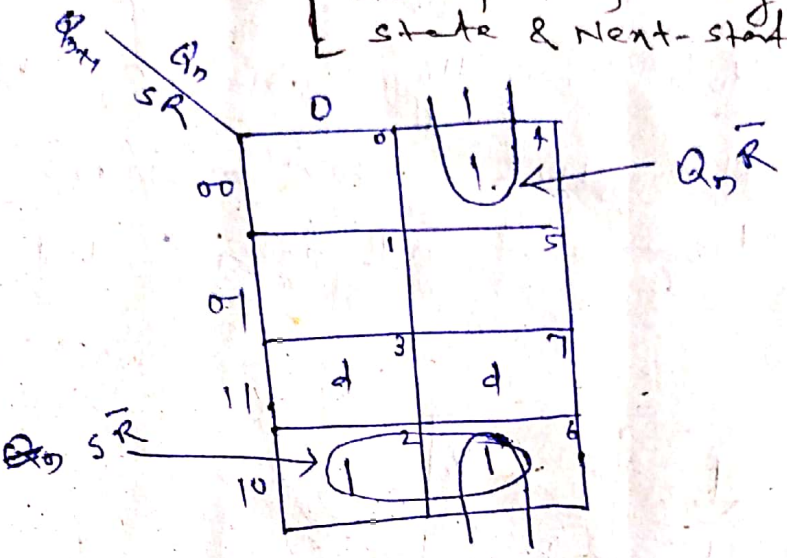
Q_n	S	R	Q_{n+1}	Action
0	0	0	0	NC
0	0	1	0	Resent
0	1	0	1	set
0	1	1	?(d)	Forbidden
1	0	0	1	NC
1	0	1	0	Reset
1	1	0	1	set
1	1	1	?(d)	Forbidden

Application or Excitation table :-

Q_n	Q_{n+1}	Excitation	
		S	R
0	0	0	d(0,1)
0	1	1	0
1	0	0	1
1	1	d(0,1)	0

When we express Q_{n+1} ~~by~~ in terms of Q_n, S, R by using k-map, thus obtained equation is called characteristic eq^n of S-R latch.

[Characteristic eq^n is developed by using Present state & Next-state table]



From k-map —

$$Q_{n+1} = S\bar{R} + Q_n\bar{R} = (S + Q_n)\bar{R}$$

This eq^n is called characteristic eq^n.