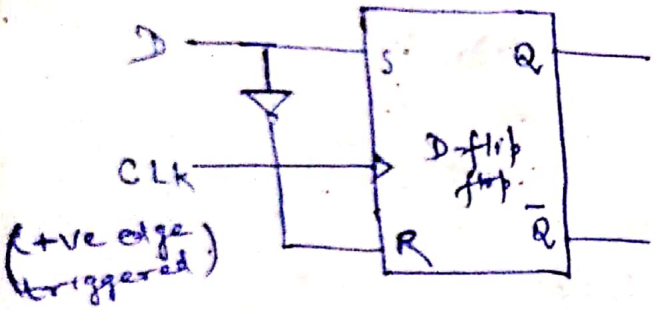
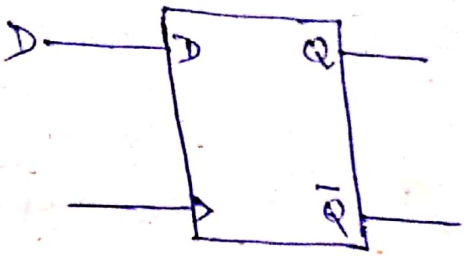
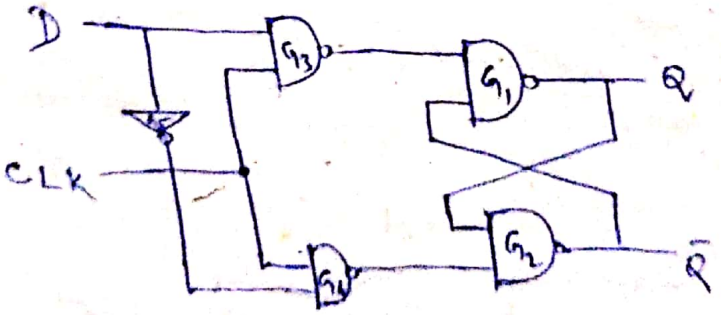
iii) D-Latch and D-flip-flop :- D or Delay flip-flop has one input and two output lines. When an inverter is connected betⁿ S and R input line of S-R flip-flop, thus obtained flip-flop is called D-flip flop. D-flip-flop basically consist of two NAND gates. The fig. as given below shows the block diagram and logic ckt of D-flip-flop.







Truth table ——

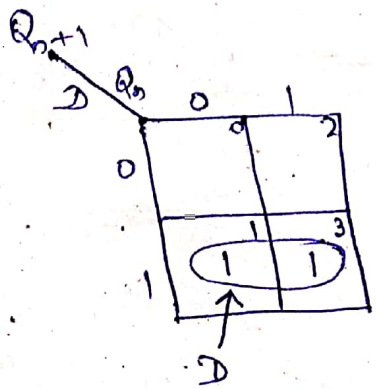
CLK	D	Q_{n+1}	Action
0	0	Q_n	NC
0	1	Q_n	NC
1	0	0	Reset
1	1	1	Set

Present state - Next state table

Q_n	D	Q_{n+1}	Action
0	0	0	Reset.
0	1	1	set.
1	0	0	Reset
1	1	1	set.

characteristic eqn ——

$$Q_{n+1} = D$$

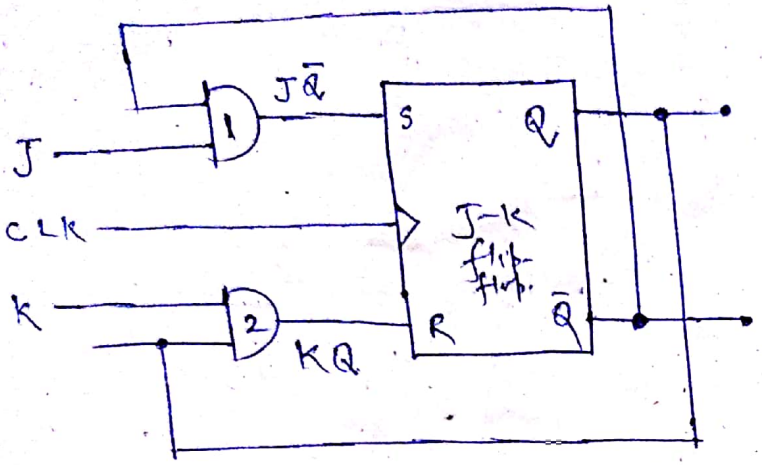


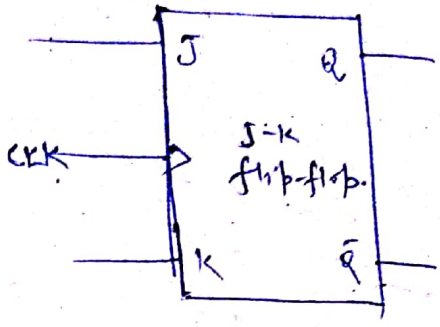
Excitation table

Q_n	Q_{n+1}	Excitation 'D'
0	0	0
0	1	1
1	0	0
1	1	1

iii) **J-K latch and flip-flop:-** J-K flip-flop is improved version of basic S-R flip-flop where the indeterminate output corresponding to S=1, R=1 has been overcome. J-K flip-flop has two inputs J and K and two outputs Q and $\bar{Q}$. A J-K flip-flop is implemented by ~~connecting J and K inputs to two AND gates~~ augmenting

two AND gates with inputs J, $\bar{Q}$ and KQ ~~as~~ to a basic S-R flip-flop as shown in fig. as below —





Block diagram.

Truth table —

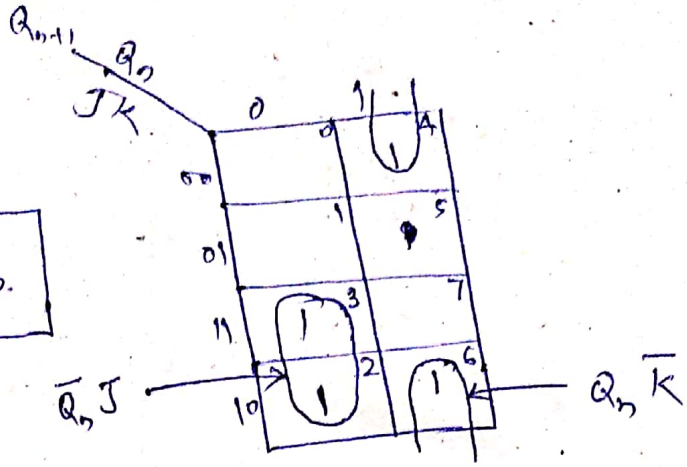
J	K	S	R	Q_{n+1}	Action
0	0	0	0	Q_n	NC
0	1	0	Q(0,1)	0	Reset
1	0	$\bar{Q}$(0,1)	0	1	set
1	1	$\bar{Q}$(0,1)	Q(1,0)	$\bar{Q}_n$	Toggle

Present state - Next state table.

	Input			
Q_n	~~Next~~ J	K	Q_{n+1}	Action
0	0	0	0	NC
0	0	1	0	Reset
0	1	0	1	set
0	1	1	1	Toggle
1	0	0	1	NC
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	0	Toggle

Characteristic eqn —

$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$



Excitation table

		Excitation I/p	
Q_n	Q_{n+1}	J	K
0	0	0	d(0,1)
0	1	1	d(0,1)
1	0	d(0,1)	1
1	1	d(0,1)	0

iv) **T-Latch and flip-flop** :- This is the flip-flop which has single input and two outputs which is obtained by using J-K flip-flop. When J and K inputs ~~or~~ lines are shorted then such a ckt gives output either No-change or 'toggle' in corresponds to the inputs 0 or 1 respectively. Hence such type of flip-flop is called T-flip-flop or toggle flip-flop. A basic block diagram is shown in fig-1

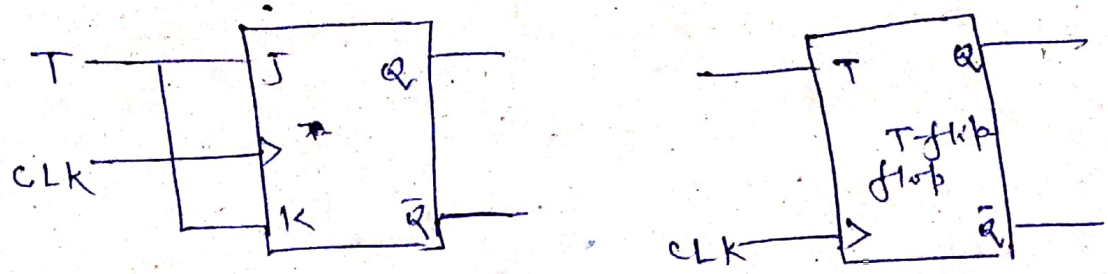


Fig-1.

Truth table ——

CLK	T	Q_{n+1}	Action
0	0	Q_n	
0	1	Q_n	
1	0	$\bar{Q}_n$	NC
1	1	$\bar{Q}_n$	Toggle.

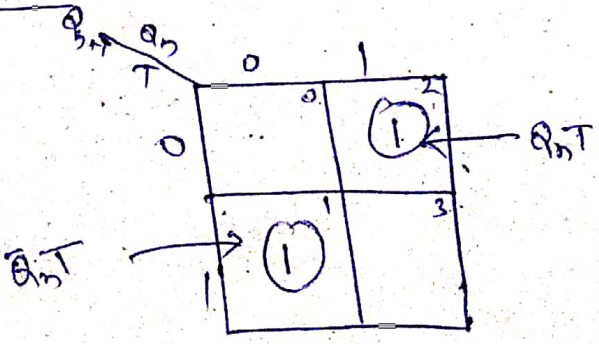
Present state - Next state table

Q_n	T.	Q_{n+1}	Action
0	0	0	NC
0	1	1	Toggle
1	0	1	NC
1	1	0	Toggle.

Characteristic eq^n ——

$$\therefore Q_{n+1} = Q_n\bar{T} + \bar{Q}_nT$$

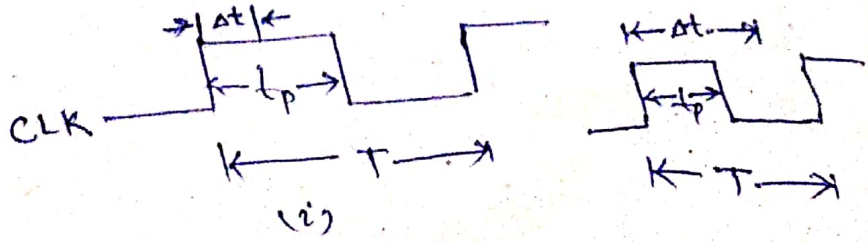
$$Q_{n+1} = Q_n \oplus T$$



v) Master-slave flip-flop :- (Discussion About ~~Ra~~ Race-around)

As we know that the operation of action of a latch is modified or controlled by applying an external clock pulse or triggering. There are two types of triggering a) Edge triggering and b) Level triggering.

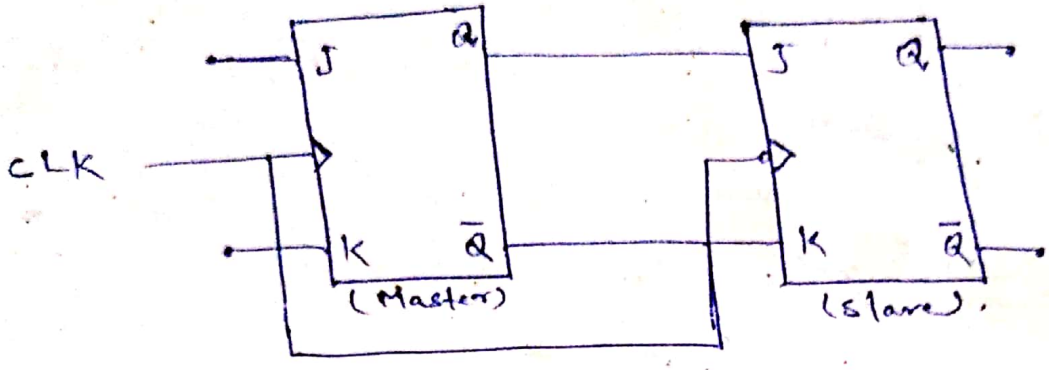
Before the development of edge triggering of flip-flop, there exist a problem in level triggering which is termed as Race-around condition. This can be understood in better way by following example. Let, us consider a J-K flip-flop is level triggered when J=K=1. Then in this case J-K excute "toggling". i.e. if previously $Q_n=0$, then $Q_{n+1}=1$ and if $Q_n=1$ then $Q_{n+1}=0$. But, there is a delay through NAND gate (propagation delay). Let a clock pulse of width t_p and period 'T' is given to J-K flip-flop to make flip-flop active



Let, 'Δt' is propagation delay time

through gate, then after delay time Δt, with $J=K=1$, output (Q) changes from 0 to 1. And, again after time Δt, output changes from 1 to 0. This back and fourth change of output from 0 to 1 and 1 to 0 takes place during ~~b~~ clock-pulse width t_p. And, hence at the end of clock pulse, the value of Q is ambiguous. This situation is called race-around condition. To remove this, $t_p \leq \Delta t < T$. This condition has been removed by Master-slave flip-flop. [OR to avoid race around cond^n, $2t_p < \Delta t < T \Rightarrow t_p < \frac{\Delta t}{2} < \frac{T}{2}$]

Master-slave flip flop :- Master-slave flip flop is constructed by using two J-K flip-flops connected as shown in fig. as below —



Master-slave J-K flip-flop

The first flip-flop which is driven by applying +ve edge triggering, is called Master and the 2nd flip-flop driven by -ve edge triggering of clock pulse is called slave. And hence entire arrangement is called Master-slave flip-flop.

When clock pulse has +ve edge, the Master operates or acts according to the J and K inputs but at that very time slave does not respond. Again, when clock pulse has -ve edge, Master flip-flop does not respond but slave acts in according to Master- previous outputs Q and $\bar{Q}$ which are inputs for slave.

A logic ckt diagram using NAND gates of Master-slave flip-flop is shown in fig. as below —