MOSFET
(Metal-oxide semiconductor FET)

MOSFET is a special type of field Effect Transistor which is also known as IGFET (Insulated Gate Field Effect Transistor). It is differed than FET on the basis of its construction and has very high input impedance of order ($10^{10} - 10^{15}$) Ω. A MOSFET is different than FET on following points ——

i) A slab of p-type or n-type is formed from a silicon base which is the foundation on which device is constructed. This is called Substrate.

ii) There are two n^+ doped (or p^+ doped) region linked by n-channel (or p-channel) named as Drain and source.

iii) Gate is insulated from conducting channel by a metal oxide film (usually SiO_2). In MOSFET, both -ve or +ve voltage can be applied to the gate.

There are two modes of operations of MOSFET ——

N-channel
- a) Deflation mode — Gate is at -ve pot^n, Drain is maintained at +ve pot^n
- b) Enhancement mode — Gate is maintained +ve pot^n, Drain " " -ve "

MOSFET

- Deflation type
  - N-channel
  - P-channel
- Enhancement type
  - N-channel
  - P-channel

[This type of MOSFET can work in both modes deflation & enhancement]

(There is diffused channel)

[This MOSFET can work in ~~both~~ only in enhancement mode because there is no continuous channel exist between source and drain]

Basic construction of n-channel Deflation-Type MOSFET :

The adjecent fig-1 shows cross-sectional view of N-channel MOSFET where a slab of P-type material (lightly doped) is formed from silicon base and is called Substrate. It is the foundation on which device is constructed. There is a metal contact SS for Substrate.

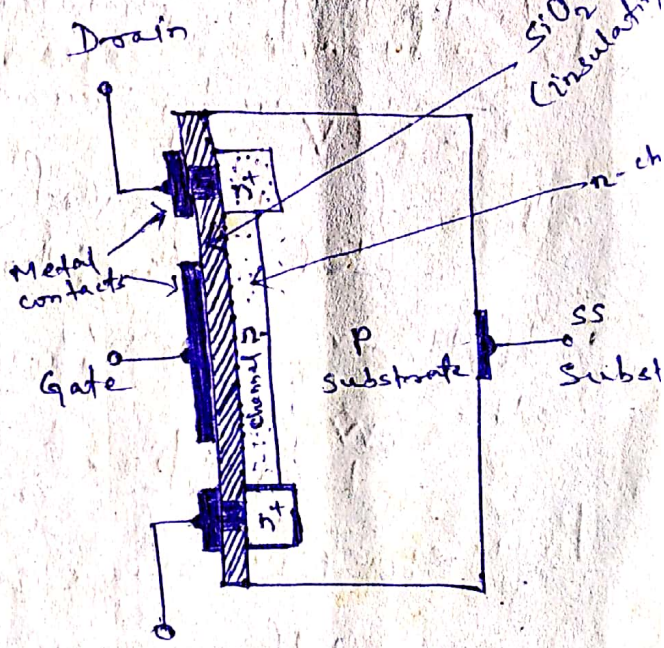


Fig-1.

(3) The two heavily doped n^+ regions are diffused into the p-substrate. These n^+ regions act as Drain and source. To this basic structure, an N-channel is diffused between source and drain as shown in fig-1. A thin layer of insulating SiO_2 is grown over the entire surface and holes are cut into the SiO_2 layer through which metal contacts (Aluminium) are made for source and drain.

On SiO_2 layer, a conducting layer overlaid covering entire channel region from drain to source. There is no any contact of this layer to channel. This layer is called Gate. Hence the device is also known as Insulated Gate Field Effect Transistor (IGFET).

Basic operation and characteristics :- ~~"DEPLETION MODE"~~ To understand the operation or working of N-channel MOSFET, here we first of all put $V_{GS}=0$ as shown in fig.2 and Drain is kept at +ve pot^n. Actually, first of all gate, source and substrate are grounded. In this case significant drain current flows for a given value of V_{DS} like a JFET. This is due to fact that when +ve pot^n is applied to drain terminal, the free electrons in n-channel are attracted towards drain which constitute the conduction of current. This current when $V_{GS}=0$, is considered as I_{DSS}. To operate a MOSFET in

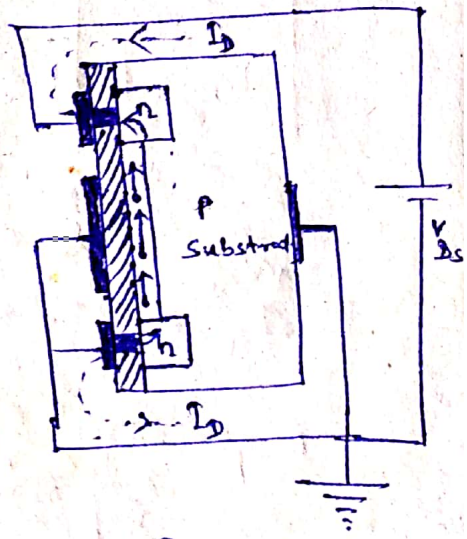


Fig-2

deflation mode we apply -ve potention to gate terminal. Now, let we apply a negative voltage at gate terminal. Due to this -ve voltage, gate will tend to pressure the electroon in n-channel towards substrate and attract the holes of p-substrate. Depending upon the negative voltage V_{GS}, a level of recombination between free electroons and holes take place which reduces the free electroon of n-channel available for conduction. As a result, the drain current reduces. The more negative voltage on gate terminal causes more deflation of free electrons of n-channel towards p-substrate and higher is the rate of recombination of electroon and holes and consequently, reduction in drain current. If V_{GS} is gradually increases negatively then at a certain value of V_{GS} no conduction takes place or in other word drain current becomes zero. This value of V_{GS} is termed as pinch-off voltage (V_P) and this condition is pinch-off or cut-off condition.

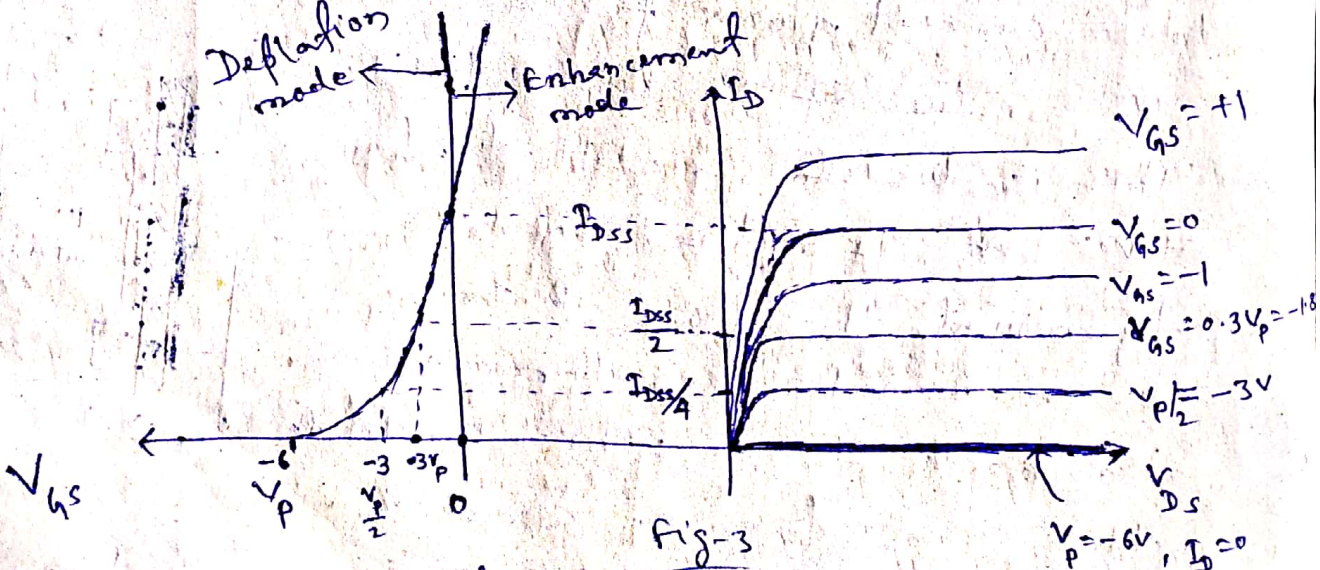


Fig-3

Transfer characteristic of N-channel MOSFET

Drain characteristic of N-channel MOSFET.

Enhancement Mode of operation:- When we apply positive voltage to this n-channel MOSFET then +ve potential at gate tend to pressure the holes of p-type substrate away from channel and attracts the minorities free electron of p-substrate towards channel due to which the most mobile charge ~~the~~ carriers which are free electrons, are available for conduction in channel. This availability of increased free electron causes to increase the drain current. If we gradually increase $V_{GS} = +1V, +2V$ and so on, the ~~good~~ drain current enhanced from I_{DSS} which is shown in transfer characteristic and drain characteristic. Thus, this mode of operation is called enhancement mode.

Depletion MOSFET transfer characteristic can be mathematically given by Shockely's eqn as below —

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Basic construction of p-channel Depletion type MOSFET

(6)

The adjecent fig-4 shows a cross-sectional view of p-channel MOSFET. For the construction of p-channel MOSFET, a slab of n-type lightly doped material is formed from silicon base on which device is constructed. This is the foundation of device and is called substrate. The two heavily doped p^+ regions are diffused into n-substrate. These regions are called drain and source. To this basic construction, p-channel is formed between source and drain by diffusion. Now, a thin layer of SiO_2 (insulating) is grown over the entire surface and holes are cut into the insulating oxide layer through which metal contacts are made for source and drain terminal. On SiO_2 layer, a conducting layer overlaid covering the channel from source to drain, this layer is termed as gate. The gate has not any contact with channel. It is insulated by SiO_2 layer. This is the cause to name the device as IGFET.

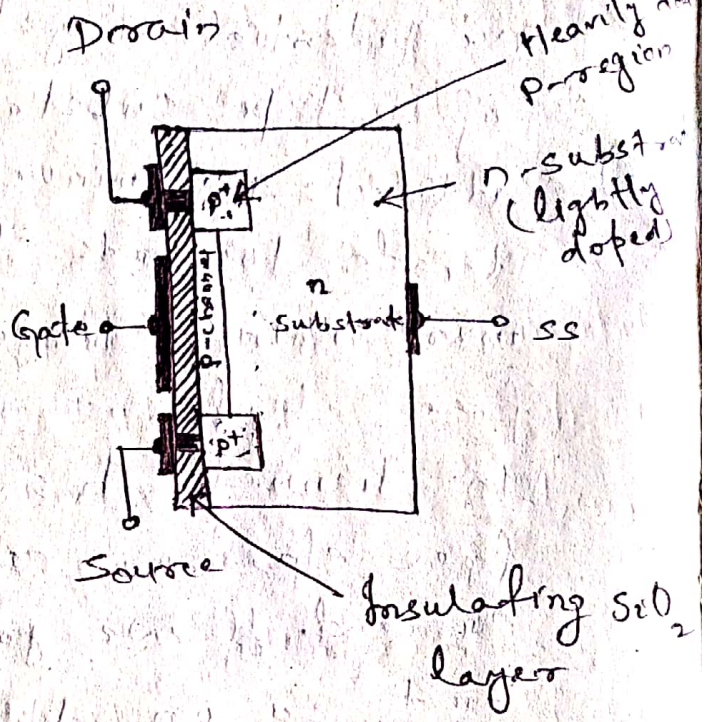


Fig-4.

Basic operation of p-channel Depletion type MOSFET :-

DEPLETION MODE of operation.

(7)

To understand the working operation of p-channel MOSFET, first of all we ground the gate, source and substrate terminal as shown in adjecent fig-5 and drain terminal is subjected to a negative potential. Due to such a connection, the holes in channel are attracted by drain terminal as the drain is at -ve potential. In this condition, for a particular value of V_{DS}, significant drain current flows. This drain current when $V_{GS}=0$ is assumed as I_{DSS}. Now, for working of MOSFET in depletion mode, we apply a +ve voltage at gate terminal. This +ve potential at gate terminal tends to pressure on holes present in channel and repel it towards substrate and attracts the free electron present in lightly doped n-substrate. ~~At a~~ Depending on the magnitude of +ve bias established by V_{GS}, a level of recombination of electron and holes take place due to which the charge carriers

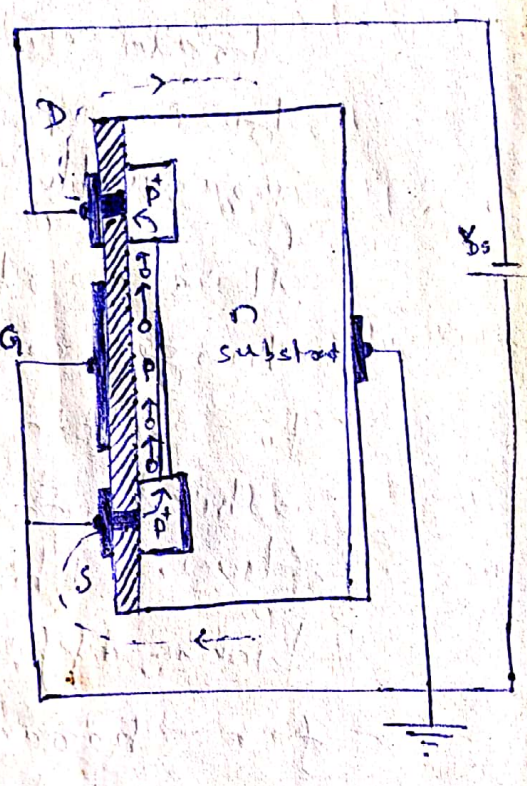


Fig-5.

in p-channel region which are available for conduction, reduces. This reduction in holes in channel causes to reduce the drain current. If we increase the gate bias voltage V_{GS} in +ve direction gradually drain current is also reduced. At a certain value of V_{GS} all the mobile charge carriers are depleted from channel to substrate and involved in recombination which results no drain current flow. This situation is known as pinch-off condition. The drain and transfer characteristic of p-channel MOSFET is shown in fig-6. as below —

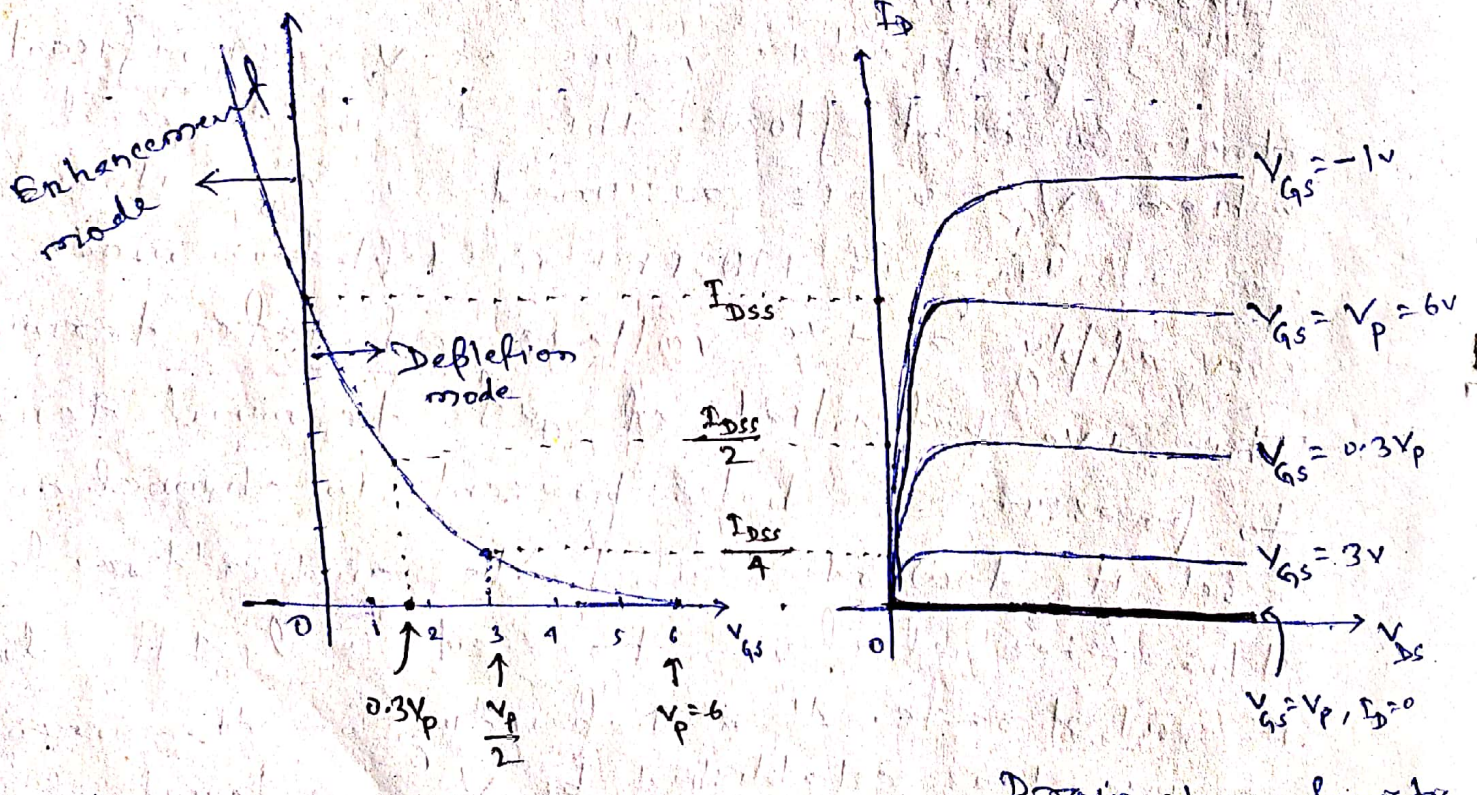
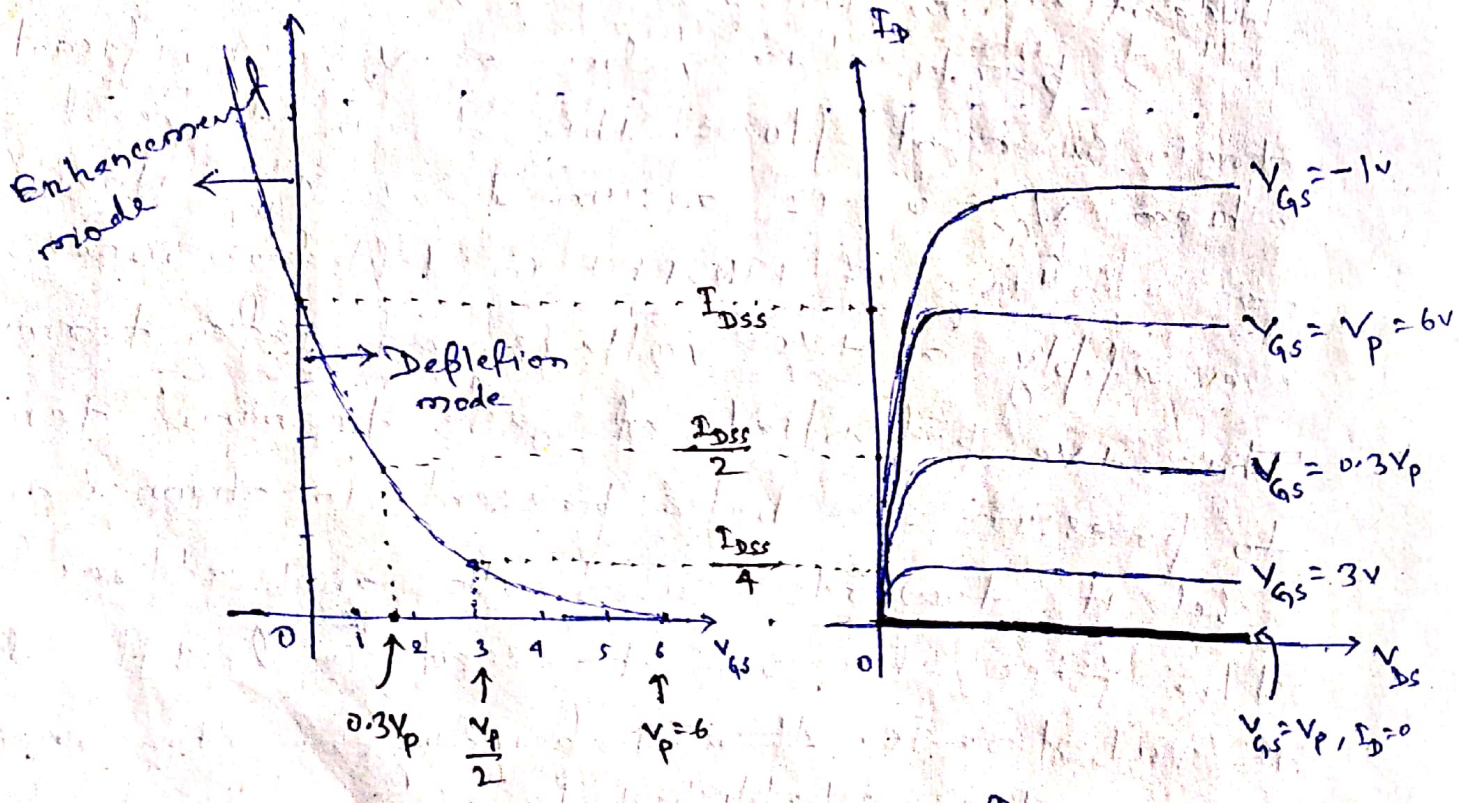


Fig-(6)

in p-channel region which are available for conduction, reduces. This reduction in holes in channel causes to reduce the drain current. If we increase the gate bias voltage V_{GS} in +ve direction gradually, drain current is also reduced. At a certain value of V_{GS} all the mobile charge carriers are depleted from channel to substrate and involved in recombination which results no drain current flow. This situation is known as pinch-off condition. The drain and transfer characteristic of p-channel MOSFET is shown in fig-6. as below —



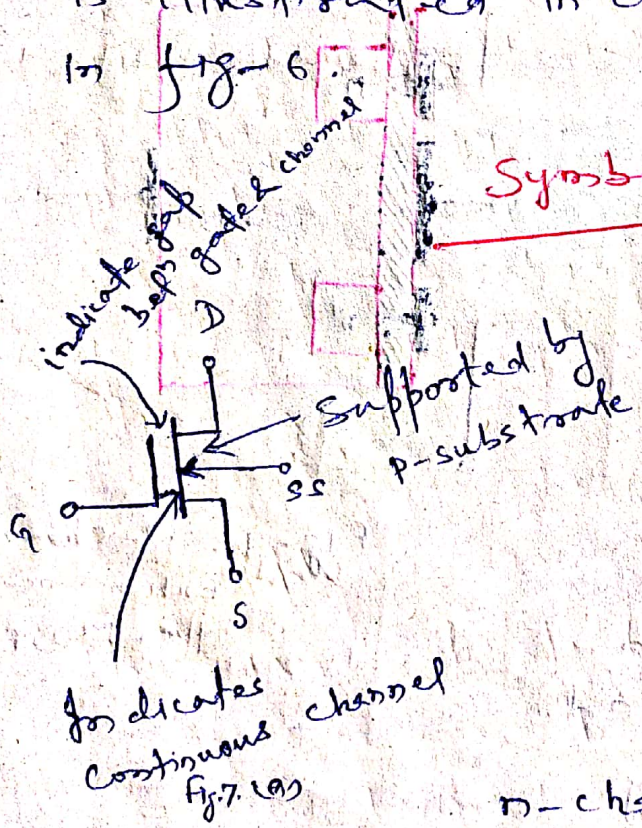
Transfer characteristic

Drain characteristic

fig-(6)

Enhancement Mode of p-channel MOSFET :- When Gate terminal is subjected to -ve potential then this -ve potential at gate terminal tends to pressure on free electrons of substrate away from channel and attracts the minorities holes of n-substrate towards p-channel due to which the holes in p-channel increase. This increase in holes available for conduction which results to increase the drain current or in other word, drain current is enhanced. Hence, this mode of operation is termed as Enhancement mode. This mode of operat^{n} is illustrated in characteristic graph in fig- 6.

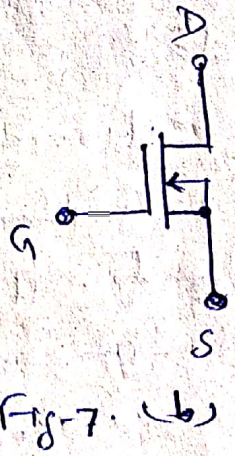
(9)

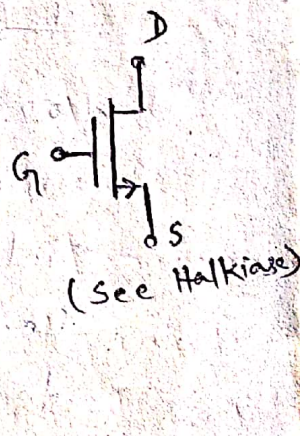


Symbole of MOSFET

indicates continuous channel

Fig.7. (a)



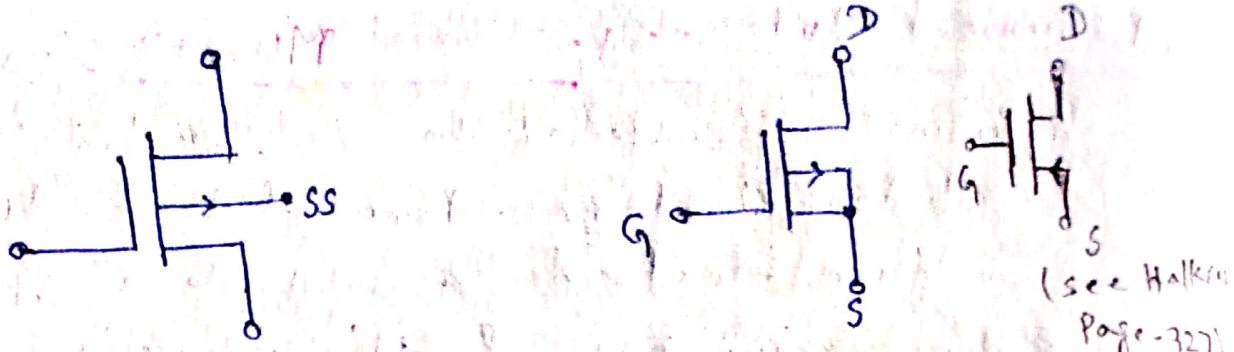


(See Halkias)

Fig-7. (b)

n-channel Deflection-type MOSFET

Sometime substrate and source terminal are internally connected. Thus in such a way MOSFET has three terminals as shown in symbole (b)



(see Halkias Page-327)

Fig-8.

p-channel depletion-type MOSFET

Enhancement type MOSFET

Basic construction of enhancement type n-channel MOSFET

The basic construction of Enhancement-type MOSFET is shown in adjecent fig-9. Here a lightly doped p-type slab is formed from silicon base and is referred as Substrate. It is the foundation on which device is constructed. Here, the two heavily doped n^+ regions are diffused into p-substrate and used as source and drain. Here, it is to be noted that there is an absence of continuous channel between drain and source. Whereas in Depletion-type

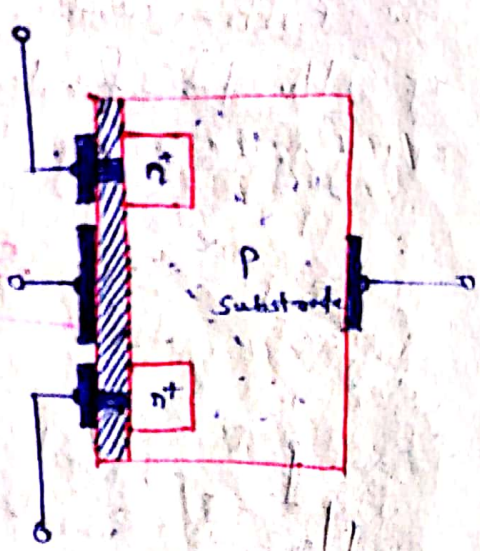


Fig-9. N-channel Enhancement type-MOSFET

MOSFET, there is always a channel betⁿ source and drain terminal. This is the basic difference between depletion type and enhancement type MOSFET. Now, an insulating layer of SiO_2 is grown over entire the surface, and holes are cut into insulating SiO_2 layer to make metallic contact for drain and source as shown in fig-9. A conducting layer overlaid on SiO_2 layer to cover the surface region between source and drain. A metallic contact is also made for this layer and used as lead but there is no any contact with substrate or doped region. This conducting layer is called gate.

Basic operation and characteristic of Enhancement n-channel MOSFET :-

To understand the working operation of n-channel MOSFET, we put $V_{GS} = 0$ volt and Drain ~~to source terminal~~ is at a positive potential as shown in fig-10. As we know that for this particular device, there is an absence of an n-channel betⁿ the region source and drain, hence there is no mobile charge carriers are available for conduction and hence no current flows through

device or we can say that $I_D = 0$. On the other hand in depletion-type MOSFET, at $V_{GS} = 0$, a significant current flows known as $I_D = I_{DSS}$

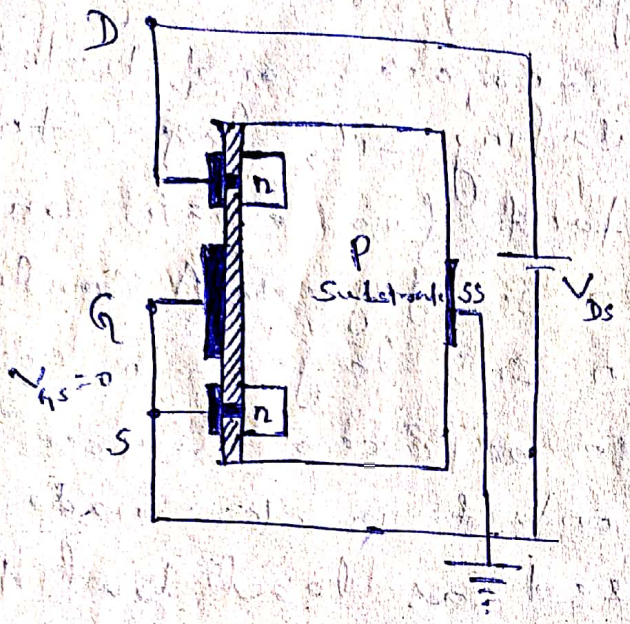
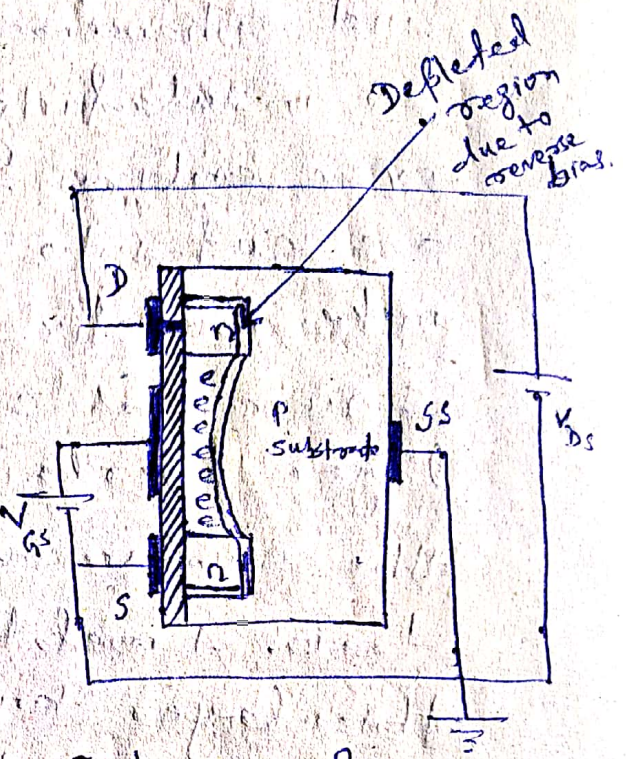


Fig-10.



Enhancement-type N-channel
Fig-11.

Now, let we apply a +ve voltage at gate greater than 0. The +ve potential at gate terminal ~~press~~ tend to pressure the holes of p-type substrate away from the region between source and drain. Along with it, this +ve pot^n at gate terminal also attracts free minorities electrons of p-substrate towards gate terminal but not accumulated at gate terminal because of insulating SiO_2 layer but it appear in the region between source and drain which now form n-channel. If we increase V_{GS} gradually the concentration of electrons near the

(13) SiO_2 layer increases. The level of V_{GS} that results the significant increase in drain current is termed as Threshold voltage V_T. Since in this type of construction, channel is non-existent at $V_{GS} = 0$ and enhanced by +ve gate to source voltage, the device is called enhancement-type MOSFET.

Both the depletion-type and enhancement type MOSFET has enhancement region but enhancement-type MOSFET is has only enhancement mode of operation.

If we increase V_{GS} more and more, the density of free electrons (carriers) increase in the induced channel. However, if we hold V_{GS} constant and increase the level of V_{DS}, the drain current will eventually reach a saturation level, as occurred for JFET and depletion type MOSFET. But, here actually there are two reversed bias p-N junctions one is at source and other is at drain terminal. Due to more +ve pot^3 at drain terminal in comparision to source terminal, there is a big depleted region at drain terminal in comperision to source terminal region.

(14) Applying kirchhoff's voltage law —

$$V_{DS} = V_{DG} + V_{GS} \Rightarrow V_{DG} = V_{DS} - V_{GS} \quad \text{——— (1)}$$

Now, Suppose we fixed V_{GS} at a certain value ~~and~~ as $V_{GS} = 8$ volt and increase V_{DS} from 2 to 5 v then $V_{DG} = 2 - 8 = -6$ to $V_{DG} = 8 - 5 = -3$.

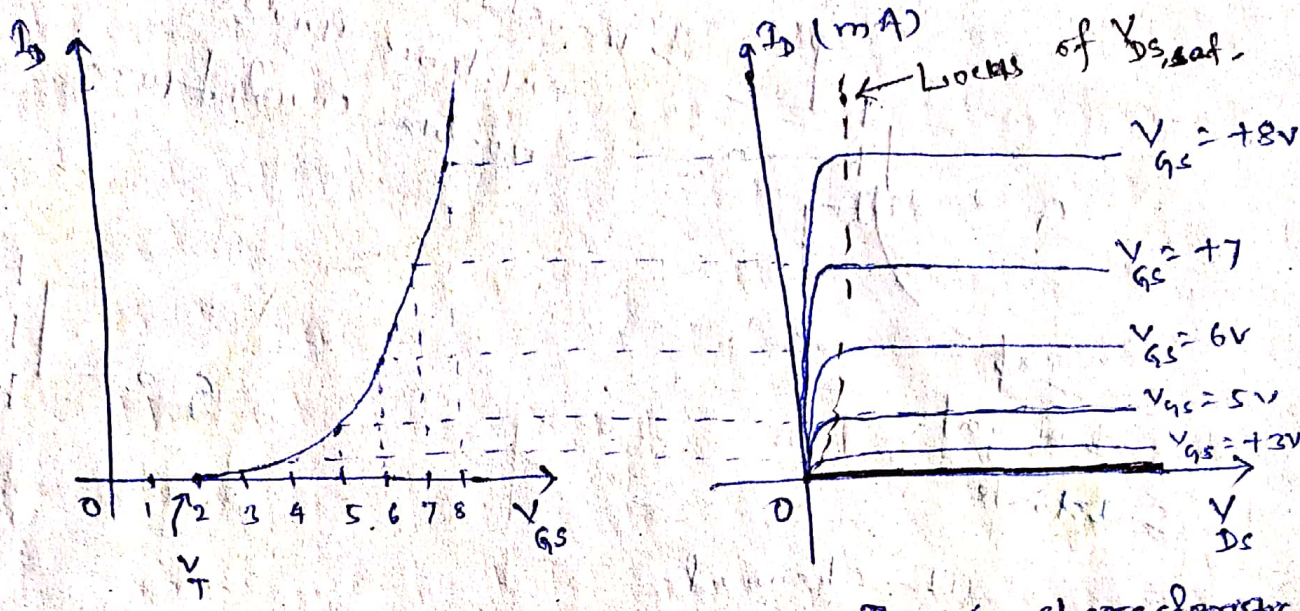
i.e,

When $V_{DS} = 2V$, $V_{DG} = -6 \Rightarrow V_{GD} = 6v$

" $V_{DS} = 5V$, $V_{DG} = -3v \Rightarrow V_{GD} = 3v$

i.e We see that if we fixed V_{GS} and increase V_{DS} (Drain to source voltage) then gate terminal become less +ve in comparision to drain. This reduction in gate to drain potential reduces the attractive forces on free carriers (electrons) in induced channel and hence width of induced channel also reduce. Eventually channel reduce to a pinch-off point and saturation level is established. In other word, any further increase in V_{DS} at a fixed value of V_{GS} will not affect the saturation level of I_D untill breakdown condition are occurred.

(15) The drain and transfer characteristic are depicted in fig-11 as below —



Transfer characteristic for n-channel enhancement MOSFET. Drain characteristic

fig-11

The saturation level of V_{DS}, is related to V_{GS} by following relation —

$$V_{DS_{sat}} = V_{GS} - V_T$$

for a level of $V_{GS} > V_T$, I_D is related with applied V_{GS} by —

$$I_D = K(V_{GS} - V_T)^2 \Rightarrow \frac{\partial I_D}{\partial V_{GS}} = 2K(V_{GS} - V_T)$$

$$g_m = 2K(V_{GS} - V_T)$$

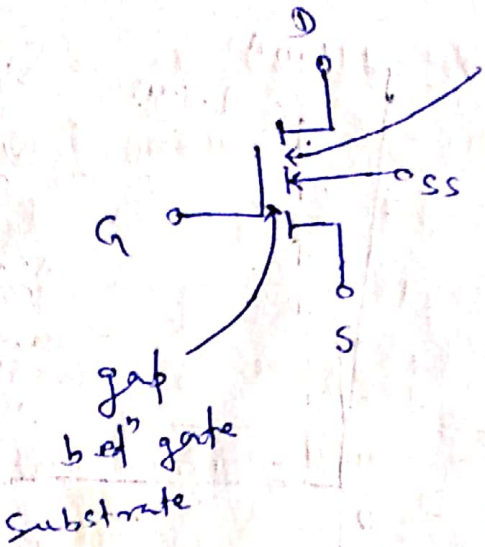
where,

$$K = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$

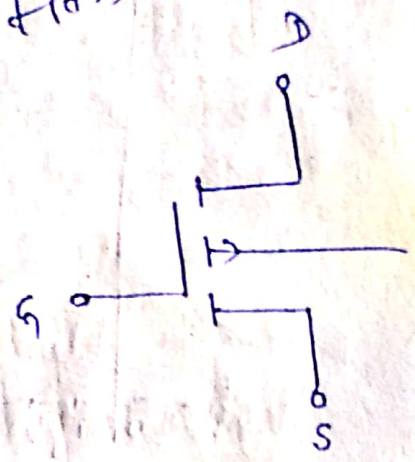
i.e. K is calculated for a particular value of (V_{GS}, I_D).

(16)

Symbols of Enhancement MOSFET



n-channel enhancement MOSFET



p-channel enhancem MOSFET.

Note:- i) For N-channel, Drain is kept at +ve pot"
ii) For p-channel " " " -ve "