① RTL (Register-Transistor Logic)

(RTL NOR gate)

A logic switching circuit (Logic-gate) constituted or consist of Resistor and Transistor (as a switch) is called RTL circuit.

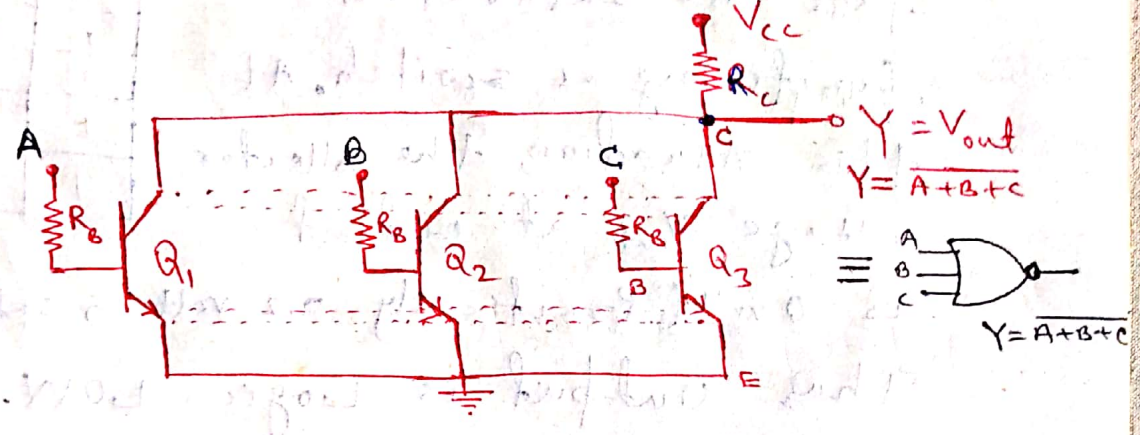


Fig-1. (RTL NOR gate)

Fig-1. shows a RTL logic circuit consist of Resistance and Transistors. Three transistors are parallel connected in CE configuration, with logic inputs — A, B, C.
To understand the ckt operation, we take following case —

Case:-I Let, all the inputs A, B, C are at logic-LOW. i.e $A=0, B=0, C=0$, then in this case, all the transistor will be in cut-off because no base current flows through transistor ($I_B=0$).

Hence $I_c=0$

At output —

$$V_{cc} = I_c R_c + V_{out} = 0 + V_{out} = Y$$

i.e Output is logic-HIGH.

Table-1.

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

case:-II. Let,

A=0, B=0, C=1

In this case, transistor-Q_3 falls into saturation functioning as switch, At this situation, the collector voltage V_{out} at output is 0 volt (Practically 0.2 volt in saturat^n). Thus Output is Logic-LOW.

case:-III. If any one input A. or B or C is at logic-HIGH, corresponding transistor comes into saturation which results output to Logic-LOW which is listed in table-1

case:-IV. If All inputs A, B, C are at logic-HIGH all transistors falls into saturation causing output to logic-LOW listed in table-1.

Thus, table-1. illustrates a truth table of 3-inputs (A, B, C) NOR gate. Hence Fig-1. represents a RTL NOR logic gate.

Here there is a point to be noted that, the resistance connected to base increases input resistance and reduces the switching speed of the circuit. This, degrades the rise and fall-time of any input pulse.

(3) To increase the speed of an RTL ckt, speed-up capacitor are connected in parallel with the base resistor as shown in fig-2.

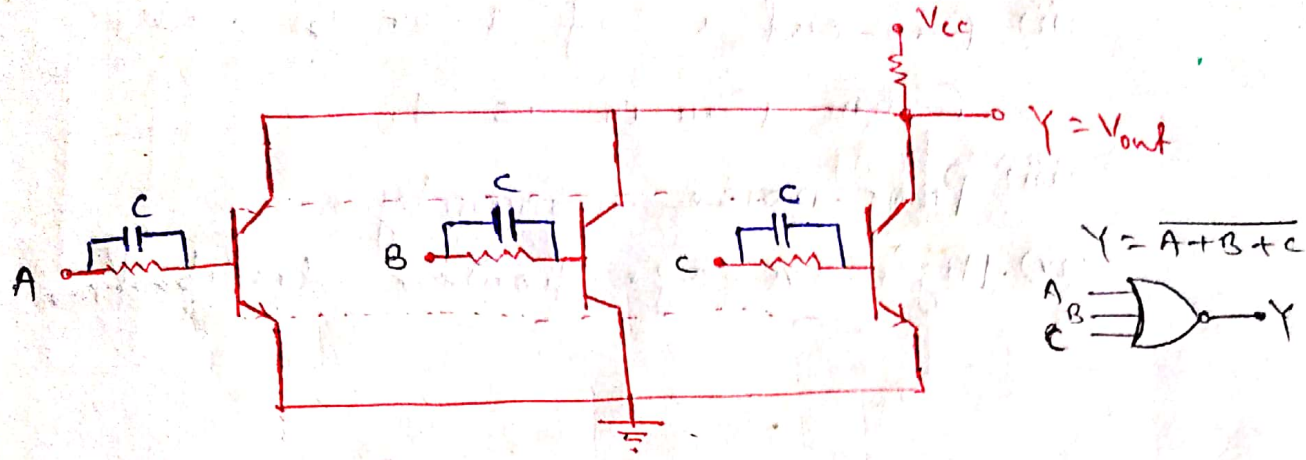


Fig-2. (RCTL NOR gate)

Here the ckt in fig-2 is also known as RCTL (Resistor-capacitor-Transistor-Logic). The capacitor connected in parallel with Base resistor, also improve the noise ~~imp~~ immunity. In this RCTL ckt, capacitor bypasses the base resistor which results the base current grow and the input capacitor discharges more quickly. The use of capacitor making possible lower power dissipation per-gate. Thus, in comparision to RTL ckt, RCTL has low propagation delay.

Advantages of RTL ckt

(i) RTL ckt is simple
(ii) Minimum number of transistor can be used.

(A)

Dis-advantages of RTL

(i) Speed of operation is Low.

(ii) Fan-out is of 4 or 5 and Fan-in is 4.

(iii) Poor noise immunity

(iv) High average power dissipation.

RTL NAND gate

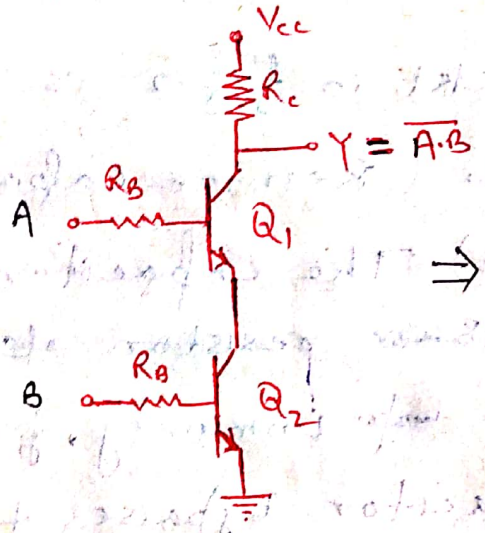


Fig-3(a)

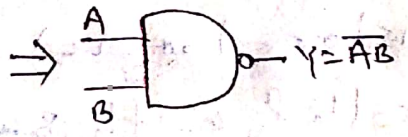


Fig-3(b)

Table-2

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Above fig-3(a) shows a RTL, 2-input NAND logic ckt. To under-stand the operation, we consider following cases —

case:-I When all inputs A, B are at logic-LOW (A=0, B=0), then no base current flows and hence, both

(5) the transistors remain in off and hence output is Logic-HIGH as listed in table-2.

case:-II. When A=0, B=1, then transistor Q_1 remain in cut-off and collector of 2nd transistor Q_2 becomes electrically isolate from supply voltage V_{cc}. Hence output, even, remain in Logic-HIGH as listed in table-2.

case:-III. When, A=1, B=0, then Q_2 remain in cut-off and hence ~~[illegible] Q_1~~, emitter of Q_1 (connected with Q_2) does not complete close ckt, which causes the output to be in Logic-HIGH

case:-IV. When, A=1, B=1, both the transistors Q_1 and Q_2 are driven to saturation, and hence, output falls into Logic-LOW.

Table-2 shows the input-output details of this RTL ckt which illustrate a NAND logical operation. Hence Fig-3(a) represents a NAND RTL logic ckt.

(6) RTL AND ckt

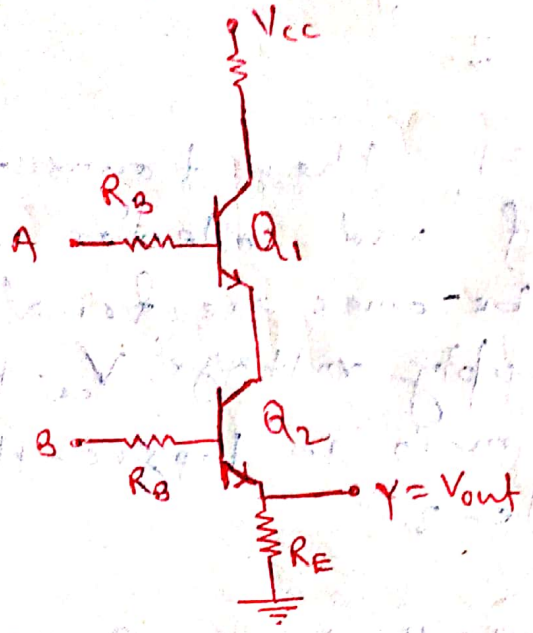


Fig - 4(a)

Table-3.

A	B	Y
0	0	0
0	1	0
1	0	
1	1	

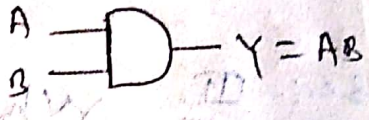


Fig - 4(b)

Fig - 4(a) shows a RTL logic ckt. To under-stand the operation, we consider following cases ——

case:-I: When, both the inputs A and B are at logic-LOW, i.e A=0, B=0, then both transistors remain in cut-off and no-base current flows through transisistor and consequently, no collector and emitter current. Due, to which output that is to be taken across emitter-load of transistor Q_2 is Logic-LOW listed in table-3.

case:-II When, A=0, B=1, then, transistor Q_1 remain in cut-off and base current flows through Q_1 results no collector and emitter current in Q_1. Consequently, transistor-Q_2 becomes electrically isolated from supply voltage V_{cc} and hence, output is Logic - LOW.

case:-III When, A=1, B=0, then no-base current flows through transistor Q_2 and comes into cut-off which results no emitter Current through R_E. Hence, Output is Logic-LOW

case:-IV. When, A=1, B=1, both the transistor ON (driving in saturation), consequently emitter current flows through R_E and there is a voltage drop across R_E. Thus, output is Logic-HIG as listed in table-3

When, we observe, table-3, it is a truth table of AND logic gate. Hence fig-4(a) represents RTL AND logic ckt

(8) # RTL NOT ckt

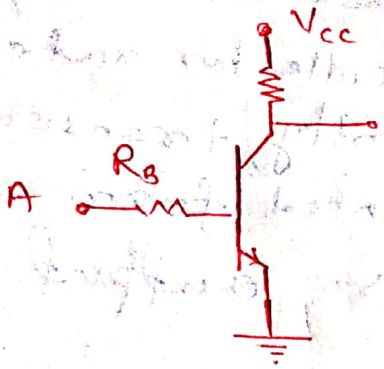


Fig-5(a)

Fig-5(b)

Table-4.

A	Y
0	1
1	0

Above fig-5(a) is a RTL logic ckt. To understand the operation, we consider following cases —

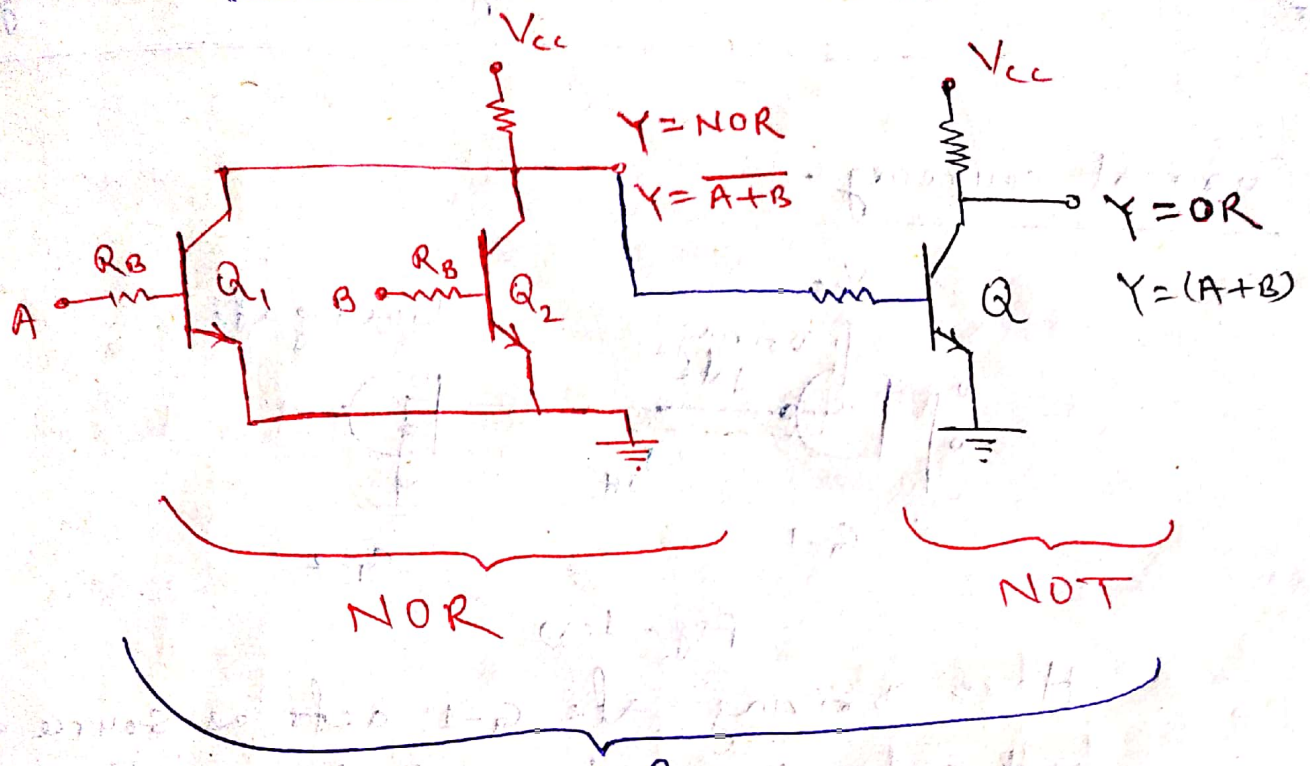
Case:-I When, A=0, Transistor remain in cut-off as there is no base current flows through transistor. Hence, output is Logic-HIGH listed in table-4

Case:-II When, A=1, transistor driving into saturation and hence output is Logic-LOW listed in table-4.

Table-4 represents a NOT operation. Hence, fig-5(a) represent RTL NOT gate.

Note:- cut-off → Logic-HIGH
saturation → Logic-LOW
} Output-side

(9) RTL OR gate



Above ckt is the composition of RTL NOR and NOT which constitutes as RTL OR logic ckt.

Current sourcing and current sinking

Current sourcing :-

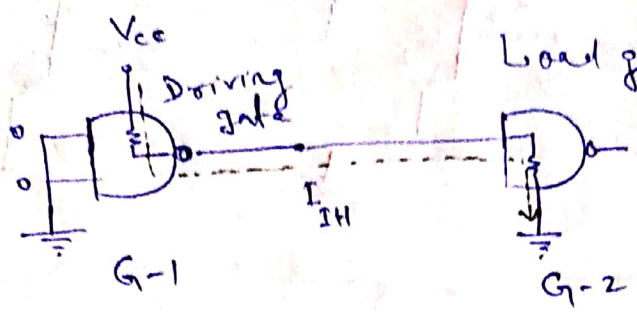


Fig- 1(a)

Here Driving gate G-1 acts as source and ~~load~~ gate G-2 acts as load. The output of G-1 is at high. It supplies current I_{IH} to the input of gate- G-1. Hence this is called current sourcing.

Current sinking :-

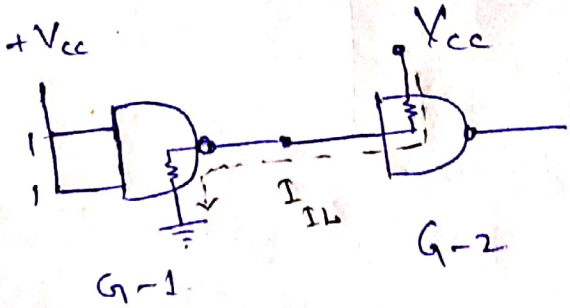


Fig-2

From above fig-2, it is clear that As soon as the output ~~of~~ Gate-G-1 goes low, current starts flowing into the output terminal of G-1 shown in fig-2. That is G-1 accepting current through o/p terminal and hence, called current-sinking take place

Multiple Emitter Transistor

A normal transistor has only three terminals — Emitter, Base and collector. But, for the logic family ckt as TTL, a special transistor constructed which has more than one emitters shown in fig-3(a) and its equivalent ckt for the convenience of analysis, is illustrated in fig-3(b). Fig-3(a) is known as Multi-Emitter Transistor.

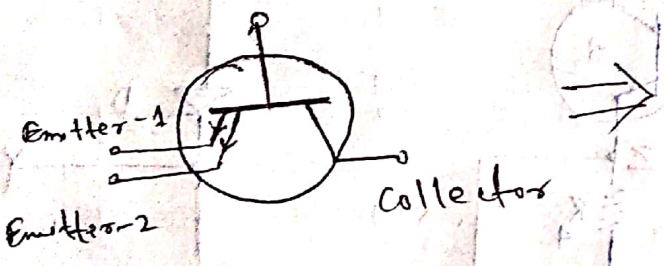


fig-3(a)

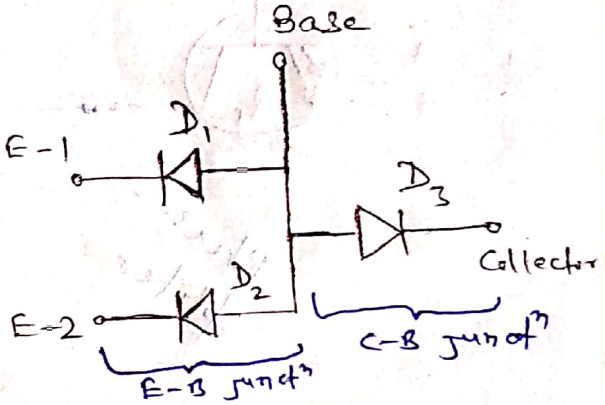


fig-3(b)

In fig-3(b), diodes D_1 and D_2 represents the two base-to-emitter junction, where as D_3 represents collector-to-base junction. This multiple-emitter transistor can be turn-ON by forward biasing either or both diodes D_1 & D_2. This transistor will be OFF state if and only if both the base-emitter junction diode D_1 and D_2 are reverse biased.

TTL Gate

TTL stands for the Transistor-Transistor Logic family. This belongs to saturated BJT logic family. Figure-1 shows a two inputs TTL-NAND gate where A and B (Multiple-Emitter terminal) are inputs and 'Y' is the output terminal.

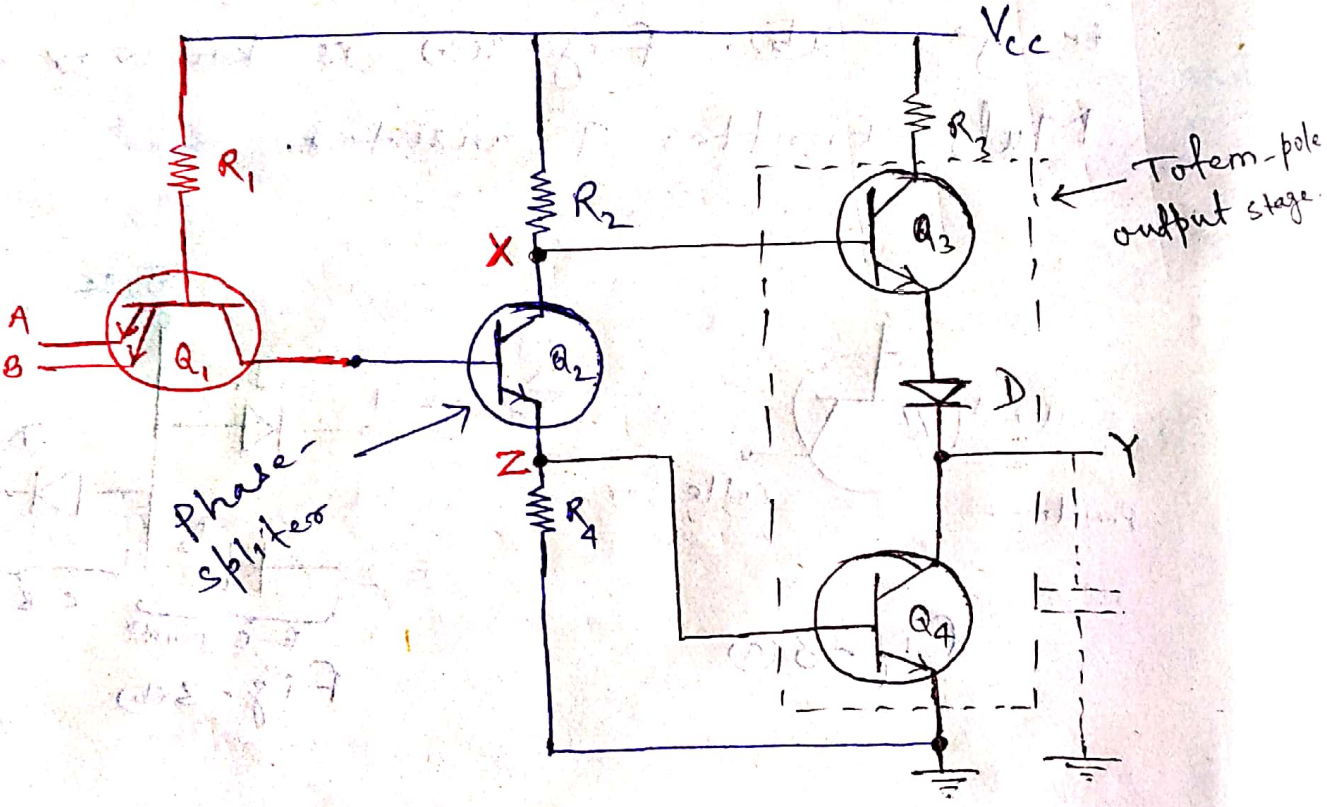


Fig-1. (Two-input TTL-NAND)

Working operation

To understand the operation, we replace multiple-emitter transistor Q_1 by its equivalent circuit diagram shown in fig-2

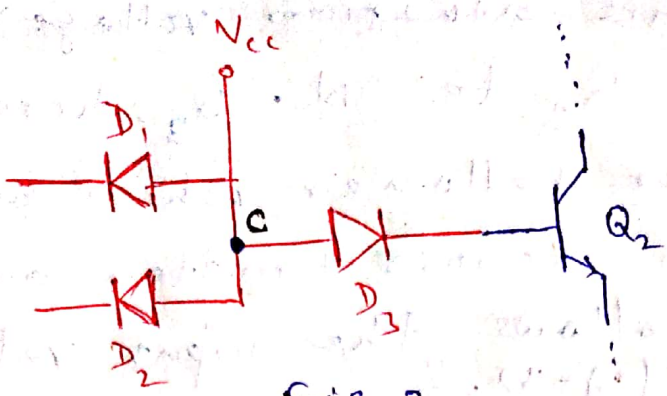


Fig-2

Case:-I . When both the inputs A and B are at logic-LOW (0), then both the diodes are forward bias and consequently B-E junction of Q_1 forward biased. In this situation, diode D_1 and D_2 (in fig-2) will conduct to force the voltage at C to 0.7 volt. This voltage is insufficient to forward bias B-E junction of Q_2. Hence Q_2 will remain in OFF. Therefore voltage at X (V_x) rises to V_{cc}. As Q_2 is off, and hence no-emitter

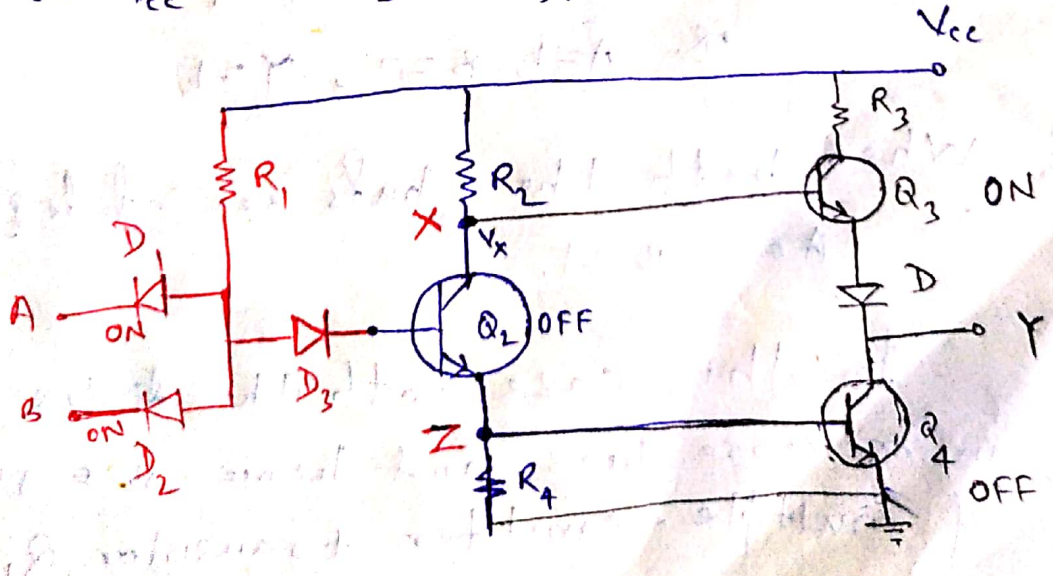


Fig-3, A=0, B=0

Current flows through Q_2 and hence $I_{B_4} = I_{E_2} = 0$, consequently Q_4 is also OFF.

But, at this situation voltage $V_x = V_{cc}$ cause to Q_3 to ON. Q_3, here functions as Emitter-follower where output is taken across Emitter and hence output follows the input voltage. (shown in fig-3).

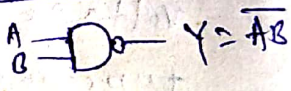
$\therefore$ A = 0, B = 0, Y = Logic-HIGH = 1

case:-II If either ~~input~~ A or B is LOW.

In this case, corresponding diode becomes forward bias and B-E junction of multiple-emitter transistor conducts, and same phenomena takes place as in case-I.

Table-1.

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



Thus, when, A = 0, B = 1, Y = 1

or, A = 1, B = 0, Y = 1

case:-III When, both the inputs are at logic-HIGH, i.e A = 1, B = 1.

In this, case, both the diodes will be in reverse bias and hence B-E junction of multiple-emitter transistor Q_1 also in reverse biased. But, at this instant diode D_3 is forward bias (collector-Base junction of Q_1) and base

(15) Current is supplied to transistor Q_2 (also called phase-splitter) via R_1 and D_2 as shown in fig-4.

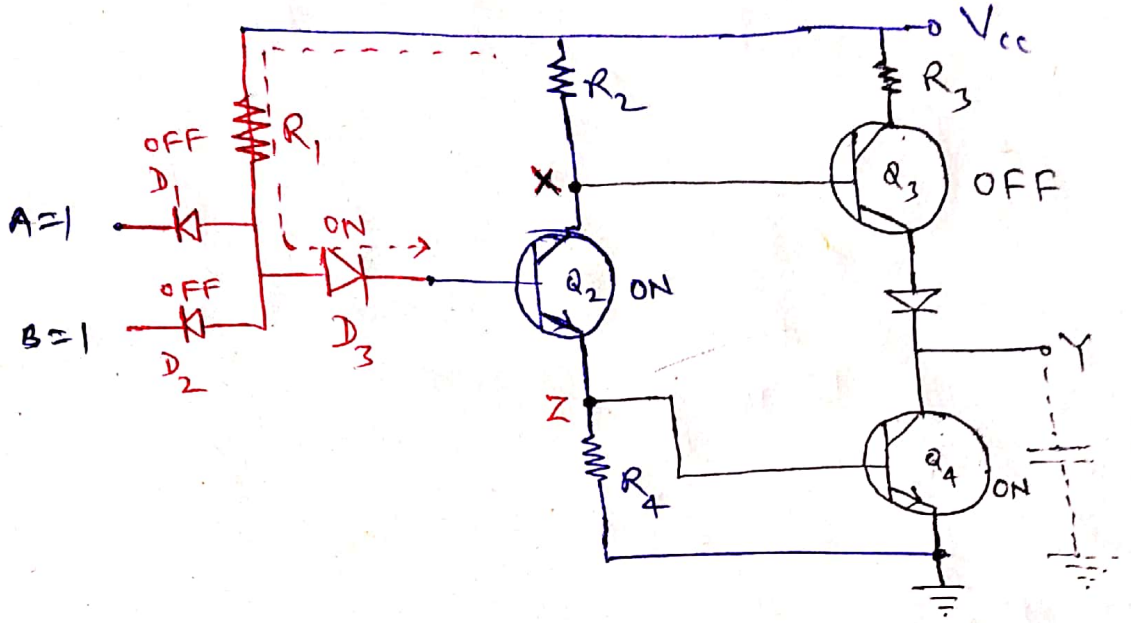


Fig-4.

As Q_2 conducts in saturation state, the voltage at point X goes down (0.2v or zero volt), the transistor Q_3 goes to OFF because, 0.2V is not sufficient to make it ON. Whereas, at same instant, voltage at Z drop across R_4 will causes the transistor Q_4 to ON (Because, Q_2 is ON and flows large emitter current I_{E_2}). As the Q_4 goes to saturation, the output voltage at point Y becomes logic-LOW. i.e A=1, B=1, Y=0.

When, we list all these input-output as in table-1, it exhibits a NAND operation. Hence ckt shown in fig-1 is a TTL-NAND logic gate.