Analog to Digital Converter (A/D converter) :-

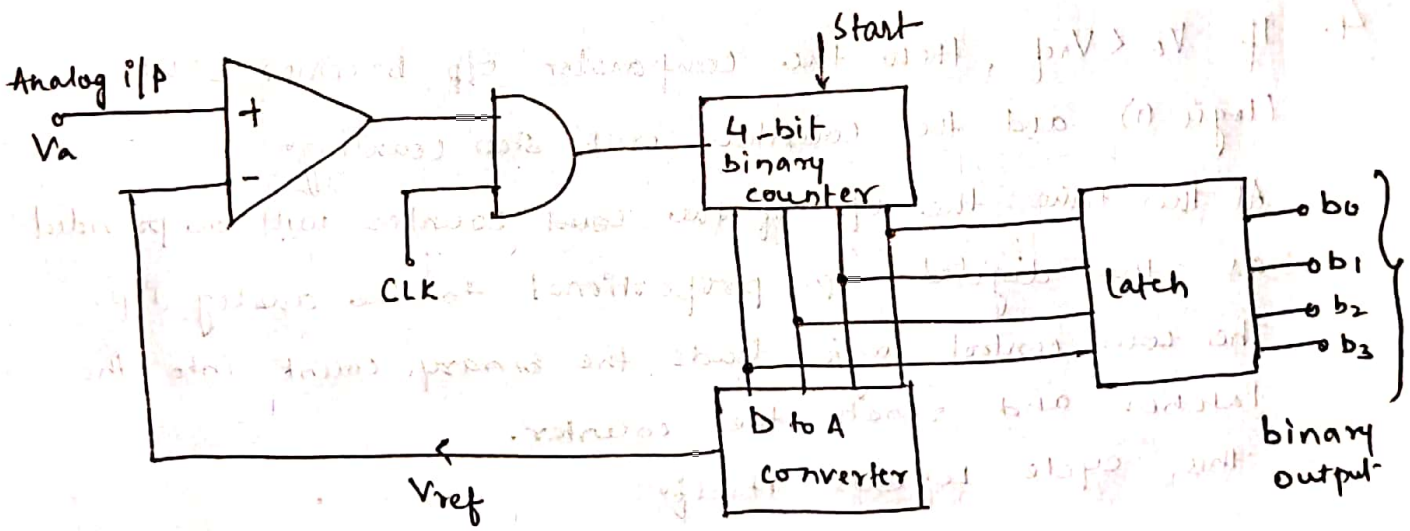
- It is often required that data taken in a physical system to be converted in digital form.

Thus, an analog to digital converter produces a digital o/p that is proportional to the value of i/p analog signal.

1. Counter type ADC :-

- simplest type of ADC. which employs a binary counter, an analog comparator, a control circuit (AND gate) and a DAC.

- also known as a digital ramp ADC, because the waveform at the o/p of the DAC is a staircase waveform (step-by-step ramp).



Operation:-

1. In a counter type ADC, the analog voltage (V_a) which is to be converted is applied to the non-Inverting terminal of the comparator. The output from the DAC (V_{ref}) is applied to the inverting terminal of the Op-Amp.

2. The counter is used to count the no. of clock pulses applied. A start pulse is applied to reset the counter to zero. initially $V_{ref} = 0$.

3. When ever the analog I/p signal is greater that the reference voltage provided by DAC, the o/p of the comparator become HIGH (logic 1), the AND gate is enabled and so, the clock pulses are transmitted to the counter

4. If $V_a < V_{ref}$, then the comparator o/p becomes LOW (logic 0) and the counter will stop counting.
At this time the o/p of the ~~count~~ counter will be provided as the digital o/p proportional to the analog I/p.
The ~~conv~~ control logic loads the binary count into the latches and resets the counter.
this cycle repeats itself.

Conversion time:-

The conversion time is the time interval b/w the starting of the conversion and the time when comparator (op amp) o/p is Low. (stopping the count).

$$(t_c)_{max} = (2^N - 1) \times t_{clk}$$

Average conversion time = $\frac{t_c(max)}{2}$.

where, N = No. of bits in the counter.

- The max^m no. of clock pulses required for n-bit conversion = $2^N - 1$
- the conversion time depends upon P/p analog voltage Va.

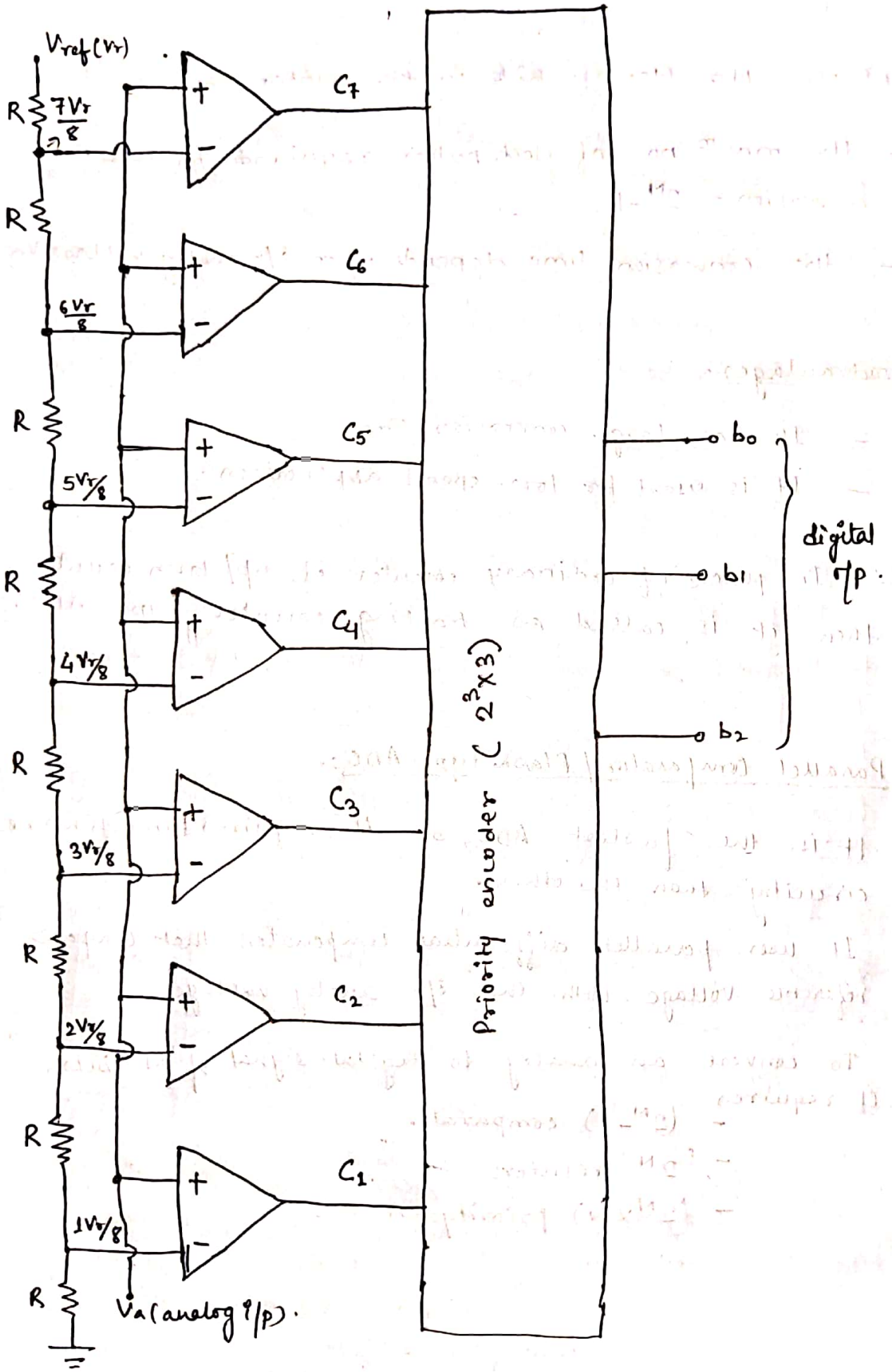
Disadvantages :-

- It has large conversion time
- It is used for low-speed application.

Note :- In place of ordinary counter if up/down counter then it is called as tracking counter type ADC.

2. Parallel Comparator / Flash type ADC :-

- It is the fastest ADC, but it requires much more circuitry than the others.
- It uses parallel differential comparators that compare reference voltage with the i/p analog voltage.
- To convert an analog to digital signal of 'N' bits, it requires
  - $(2^N - 1)$ comparator
  - (2^N) resistors
  - $(2^N \times N)$ priority encoder



Above figure shows a 3-bit flash type A/D converter which requires.
- $(2^3-1) = 7$ comparators.
- $2^3 = 8$ resistors
- $2^3 \times 3 = 8 \times 3$ priority encoder.
  (i/p: 8, o/p: 3)

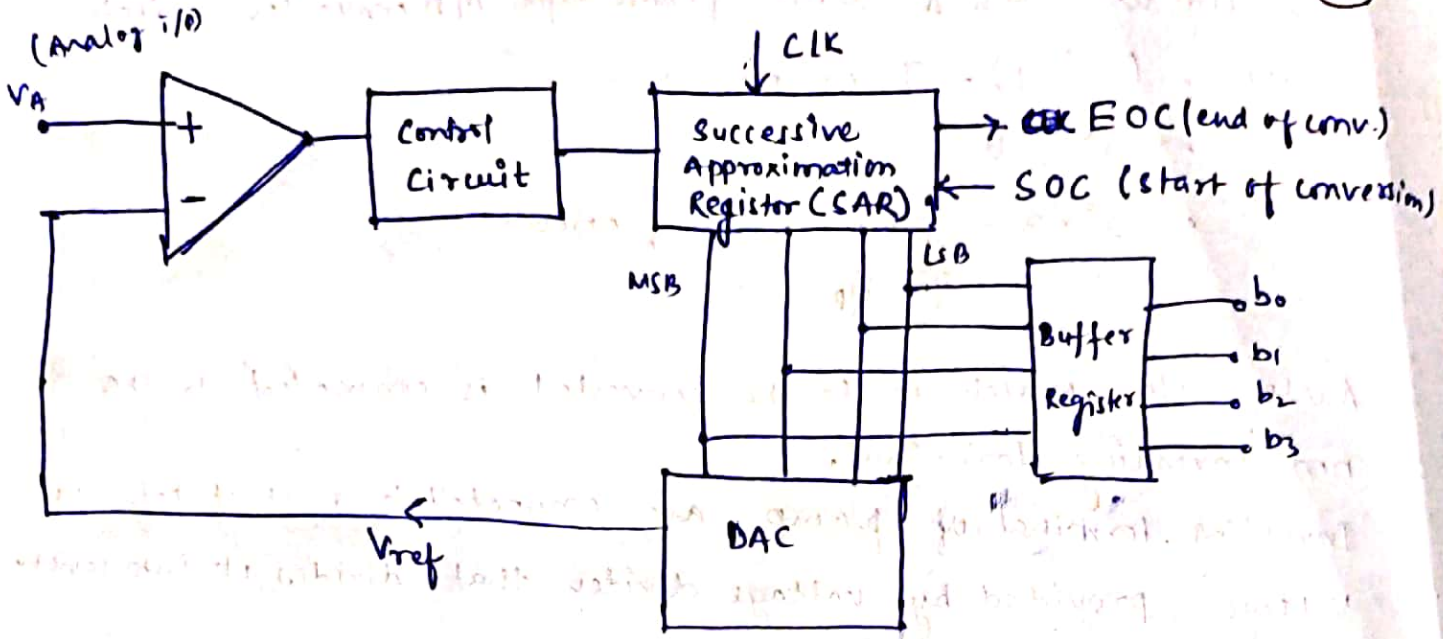
- Analog i/p which is to be converted is connected to the non-inverting terminal.
Inverting terminal of op-amp, are connected to a set of reference voltage provided by voltage divider that divides it into seven equal increment levels.

- All comparator o/ps are connected to a priority encoder, which produces a digital o/p corresponding to the i/p having highest priority.

- Flash converter uses no clock signal. The conversion takes place continously. Thus, the max^m no. of clock pulses required for conversion is '1'.

3. Successive Approximation type ADC:

- one of the most widely used types of A/D converter.
- the conversion time of this converter is maintained constant and it is proportional to the no. of bits in the digital o/p.
thus, tc is independent of the value of analog i/p voltage (V_A).
- The basic working principle of this converter involves the approximation of analog i/p voltage against N-bit digital value using 1 bit at a time, begining with MSB.



- Above figure shows as block diagram of 4-bit successive approximation type ADC.

Operation:

1. The bits of digital to analog converter are enable one at a time (begining with MSB). As each bit is enabled, the comparator produces an o/p.

2. If $V_{ref} < V_a \Rightarrow$ comparator o/p : high, the MSB is retained as 1 and next MSB is set to 1.

   And, if $V_{ref} > V_a \Rightarrow$ comparator o/p low, the MSB is set to 0 and the next MSB is set to 1.

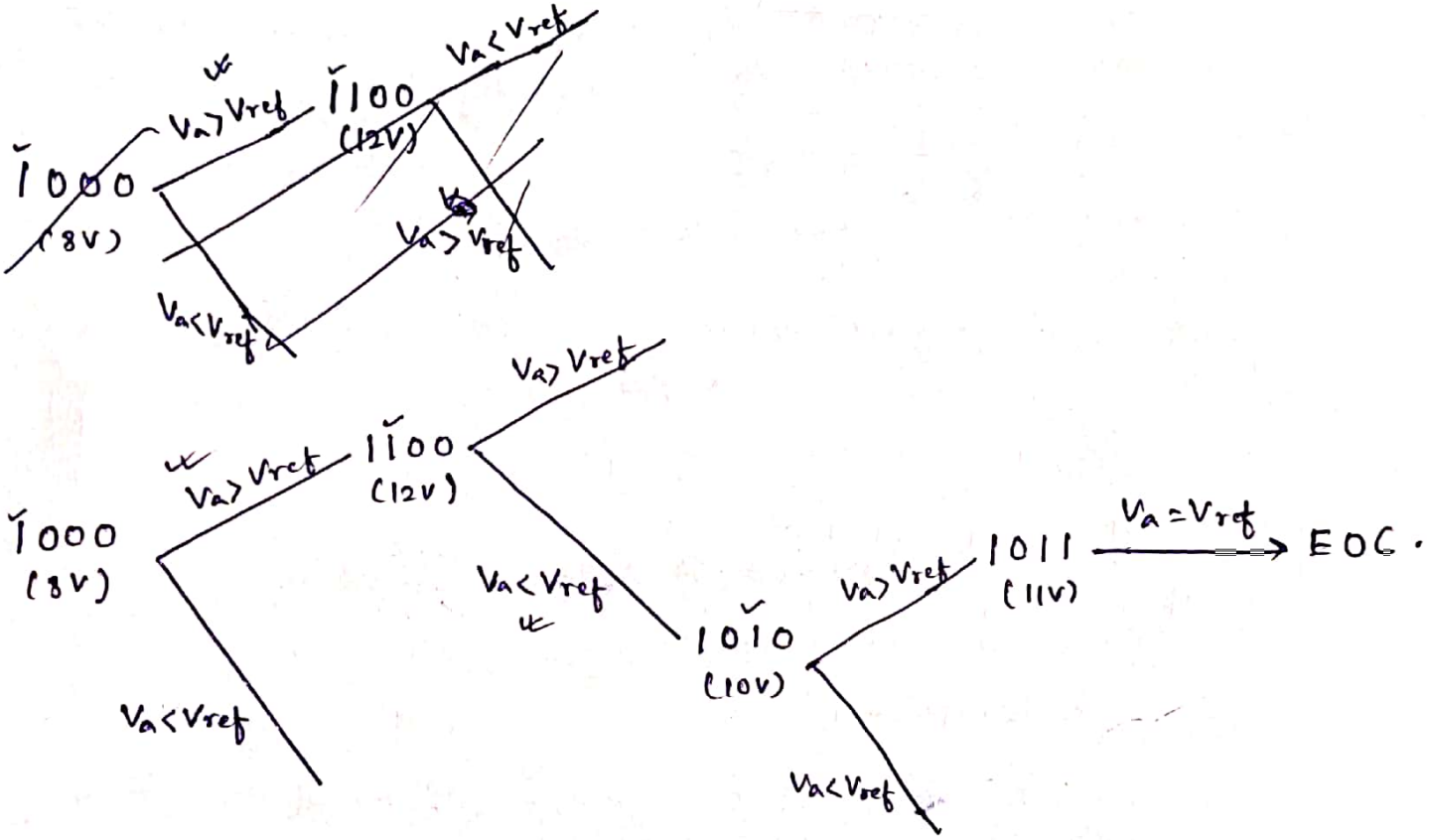
3. After the end of conversion EOC signal is enabled and the digital equivalent is loaded as the output.

Let's take an example to understand the operation :-

Let's take $V_a = 11V$.

First, MSB is set to 1 and all the other bits are 000.

i.e $V_{ref} = 1000$
decimal equivalent = 8 V



Conversion time (t_c) :-

$$t_c = N \times t_{clk}$$

Note :-

1. In SAR type ADC, ring counter is used to successively set the bits.
2. SAR type ADC is mostly used in digital circuits to provide interfacing with microprocessor.

Specifications of A/D converter:-

- Range of i/p voltage = $V_{max} - V_{min}$.
- ~~Resou~~ Resolution = $\frac{V_{max} - V_{min}}{2^N - 1}$

$$\% \text{ resolution} = \frac{1}{2^N - 1} \times 100\ \%$$

- Dynamic range = $(1.76 + 6N)$ dB