Analog to Digital Converter (ADC)

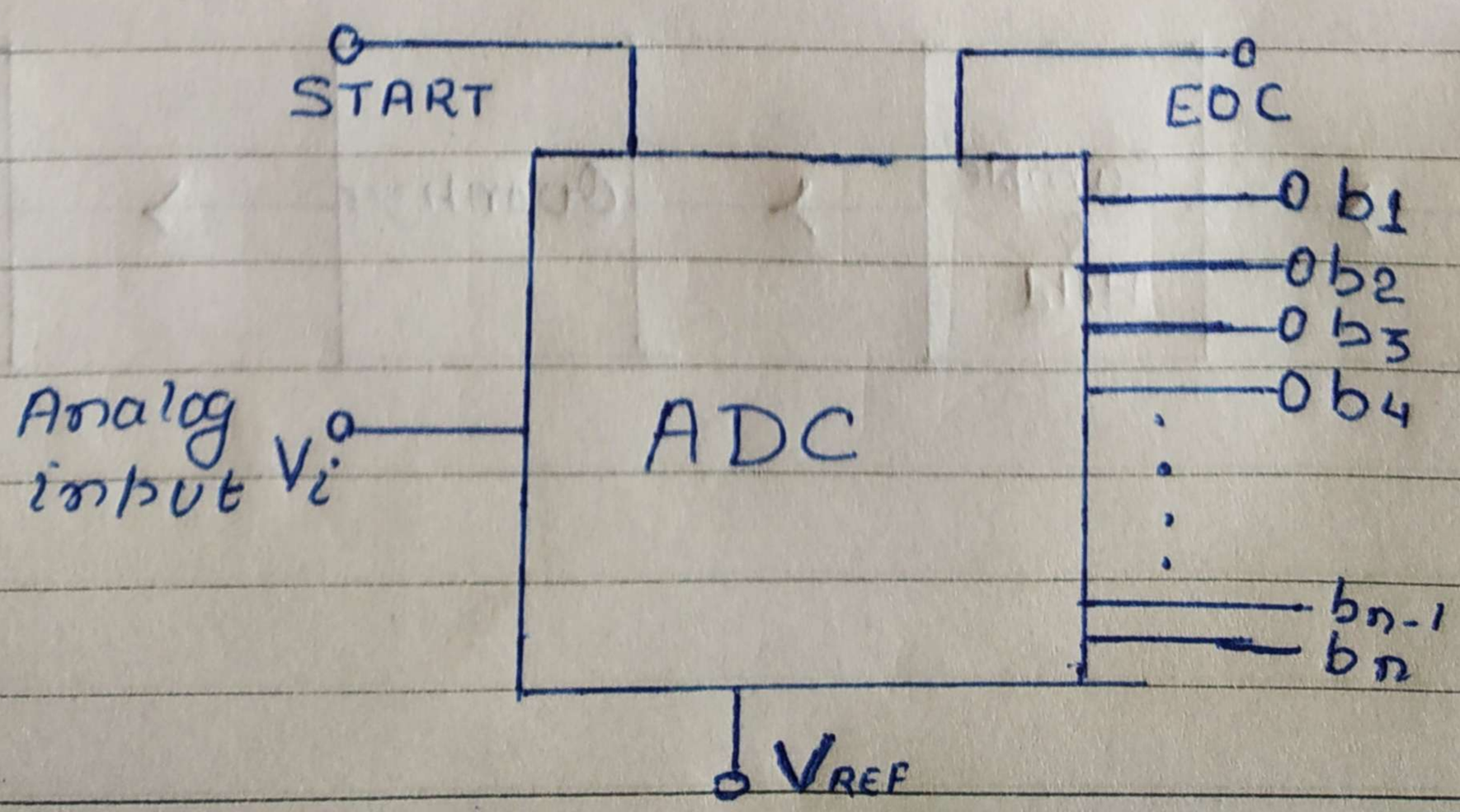
An Analog to Digital Converter does the inverse function of DAC. It converts an analog signal into its equivalent n-bit binary coded digital output signal. The analog input is sampled at a frequency much higher than the maximum frequency component of the input signal. The digital output from an ADC can be Serial or parallel form.

The ADC accepts an analog input V_i and produces an output binary word $b_1, b_2, \cdots b_n$ of fractional value D such that

$$D = \frac{b_1}{2} + \frac{b_2}{2^2} + \cdots + \frac{b_n}{2^n}$$

where b_1 is MSB and b_n is LSB.

The Symbolic representation of an n-bit ADC is shown in figure.



Two additional control pins START input and End of Conversion (EOC) output are provided with ADC. The START input initiates the conversion and the EOC announces when the conversion is complete. The output can be of parallel or serial form. Usually latches, Control logic and buffers are provided to enable interfacing of the ADC to microprocessor or LCD/LED display directly.

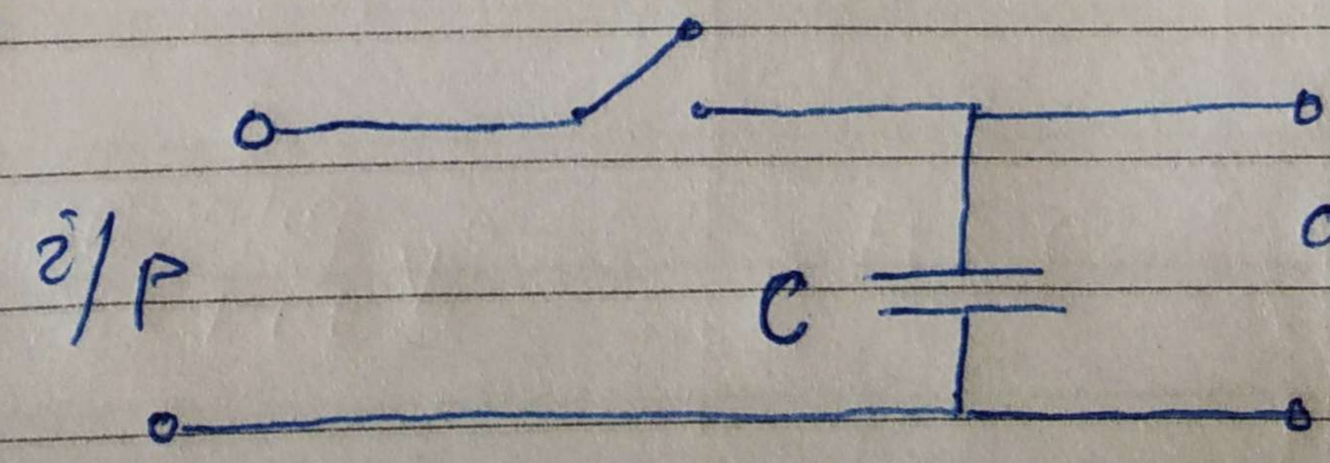
The ADC conversion process divides the analog input into 2^n intervals. These intervals are called code ranges and all the values of v_i falling with'n a code range are represented by the particular code.

The general block diagram of ADC converter is shown below

The prefliter avoids the aliasing ~~signal into~~ of high frequency signals. When a signal fi is sampled at a rate lower than $2f_i$, aliasing error occurs. The aliasing error is a phenomenon in which, the frequency appear to be different from their true values and the signal cannot be recovered correctly.

It is not always possible to exactly identify the frequency content of random data signals. Therefore, it is a common practice to pass the analog signals through a low pass filter known as pre-filer before sampling. The filter characteristics are such that it can reject all components equal to or greater than half the sampling rate.

The Sample-and-Hold circuit holds the input analog signal into the ADC at a constant value during the conversion time. Its circuit diagram is given as



The quantizer segments the reference voltage signal into subranges. For n-bit digital output code, there are 2^n subranges. The digital processor or encoder forms the encoder circuit which encodes the subrange into the corresponding digital bits.

13.8 SPECIFICATIONS OF A/D CONVERTER

Some important specifications, namely, accuracy, differential linearity, conversion time, input voltage range and resolution of A/D converters are discussed below.

Resolution

The *resolution* refers to the finest minimum change in the signal which is accepted for conversion, and it is decided with respect to the *number of bits*.

It can be defined as *resolution* = $1/2^n$, where n is the number of digital output word bits. The ratio of the full-scale input voltage range V_{FS} to the resolution gives the minimum change of input voltage which can cause a change of 1 LSB at the output. This can be expressed as

$$\Delta v_i \text{ for 1 LSB} = \frac{V_{FS}}{2^n} \tag{13.18}$$

where V_{FS} is the full-scale input voltage range.

If the number of bits used to represent a signal is larger, then the resolution improves. For example, if an 8-bit word is used, a maximum of 256 distinct values are available. If a maximum analog signal amplitude of 1 V is used, then each step in the word represents $V/256 = 3.9$ mV. If 16 bits are used for the same 1 V range, then each step would produce $V/65536 = 15.26$ mV.

The digital output starts at 0 for an A/D converter. Therefore, the maximum full-scale input voltage which will cause the output to be all logic 1s is 1 LSB less than the full-scale voltage range.

$$v_{iFS} = V_{FS} - 1 \text{ LSB} \tag{13.19}$$

where v_{iFS} is the maximum input voltage which can cause all 1s at the output.

Quantization Error

A digital error in an A/D converter is based on the resolution of the digital system. In A/D conversion, a continuous analog voltage is represented by an equivalent set of digital numbers. When the digital numbers are converted back to analog voltage by a D/A converter, the output is a staircase waveform, which is a discontinuous signal composed of a number of discrete steps. The smallest digital step is due to the LSB and it can be made smaller only by increasing the number of bits in the digital representation. This error is called *quantization error*, or *digitizing error* and it is commonly the bit.

As shown in Fig. 13.13 (b) the digital output is 011 for all values of $\frac{3}{8}V \pm \frac{1}{2}LSB$. Therefore there is an uncertainty about the exact value of v_i when the output is 011.

This uncertainty is called the *quantization error* and its value is $\pm \frac{1}{2}LSB$.

Increasing the number of bits of A/D converter results in finer resolution and smaller quantization error.

Analog Error

Analog error in an A/D converter is mainly due to variations in the dc switching point of the comparator. The variations in switching are mainly due to offset, gain and linearity error of the operational amplifier used in the comparator. The other sources of analog error are the resistors in the A/D converter, the reference voltage source and the ripple and noise introduced by the circuit components.

Linearity Error

This is an important measure of A/D converter performance. It is defined as a measure of the variation in voltage step size. This indicates the difference between the transitions for a minimum step of input voltage change. This is normally specified as a fraction of 1 LSB.

Differential Nonlinearity (DNL) Error

The analog input levels that trigger any two successive output codes should differ by 1 LSB (DNL = 0) for an A/D converter. Any deviation from 1 LSB value is defined as DNL error.

The counter type and continuous type A/D converters normally have better differential linearity than successive approximation type A/D converters.

Integral Nonlinearity (INL) Error

Figure 13.15 shows an actual A/D converter characteristic with a missing code. The dotted curve represents the locus of the midpoints of the actual input step voltage ranges. This line is called the *code center line*. The maximum deviation of the code center line from the straight line passing through the end points of the ideal characteristics after nulling the offset and gain errors is called *integral nonlinearity error* (INL).

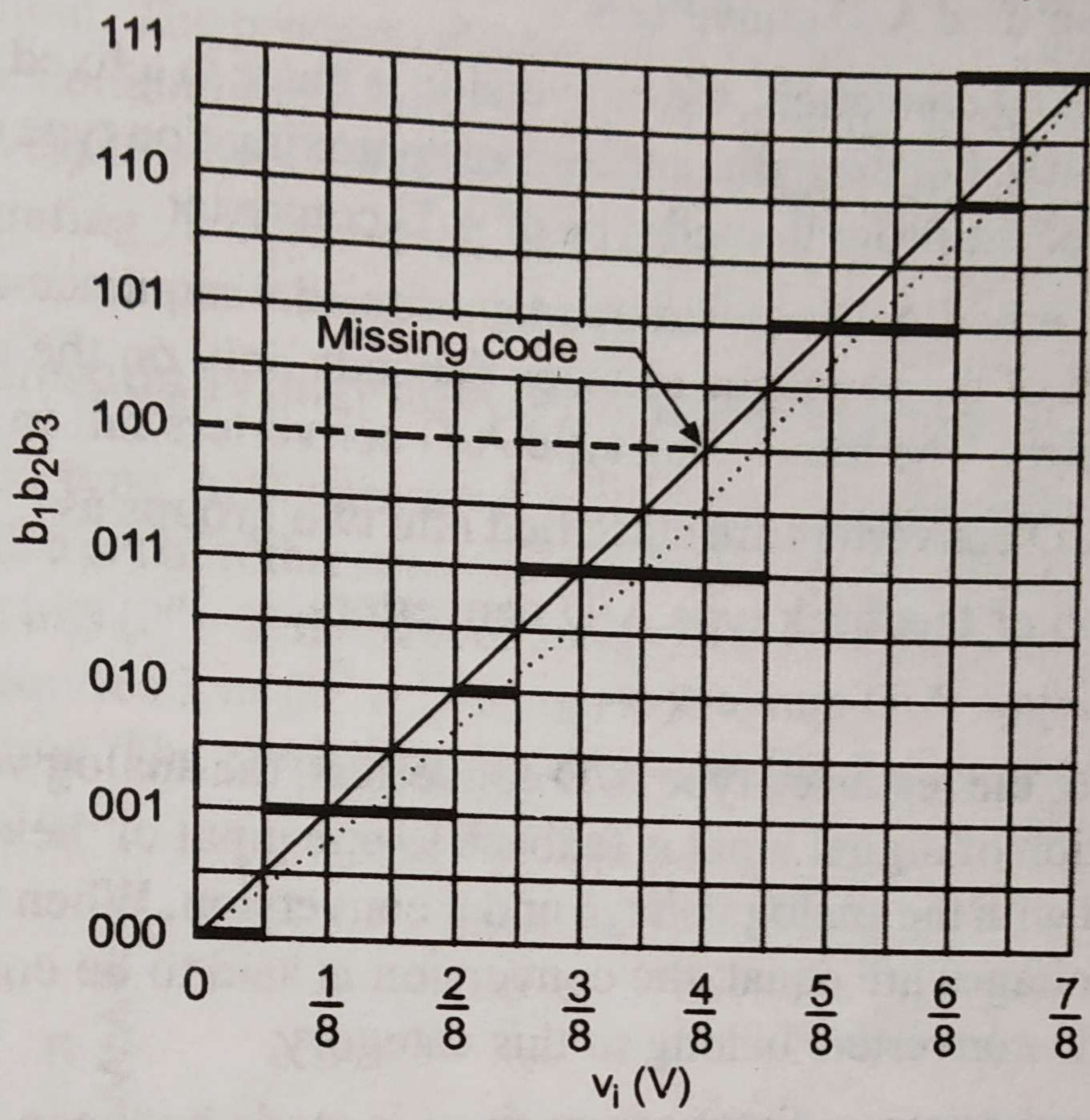


Fig. 13.15 *A/D converter characteristic with a missing code*

Dither

The performance of A/D converters can be improved using *dither* <*http://en.wikipedia.org/wiki/Dither*>. This is a very small amount of random noise (white noise <http://en.wikipedia.org/wiki/White_noise>) which is added to the input before A/D conversion. Its amplitude is set to half of the LSB value. Its effect is to cause the state of the LSB to randomly oscillate between 0 and 1 in the presence of very low levels of input, rather than sticking at a fixed value. Instead of the signal simply getting cut-off altogether at this low level (which is only being quantized to a resolution of 1 bit), it extends the effective range of signals that the A/D converter can convert, at the expense of a slight increase in noise. Thus, the quantization error is diffused across a series of noise values which is far less objectionable than a hard cut-off. The result is an accurate representation of the signal over time. A suitable filter at the output of the system can thus recover this small signal variation.

Conversion Time

The time required for an A/D converter to convert an analog input value into its equivalent digital data is called the *conversion time.*

Input Voltage Range

It is the range of voltage that an A/D converter can accept as its input without causing any overflow in the digital output.